Alberto Nannarelli - DTU Orbit (23/12/2017)

Nannarelli, Alberto
alna@dtu.dk

Department of Applied Mathematics and Computer Science - Associate Professor

Embedded Systems Engineering

Publications:

A Multi-Format Floating-Point Multiplier for Power-Efficient Operations
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

Digital Arithmetic: Division Algorithms
Publication: Research - peer-review › Book chapter – Annual report year: 2017

RNS Applications in Digital Signal Processing
Publication: Research - peer-review › Book chapter – Annual report year: 2017

Robust Throughput Boosting for Low Latency Dynamic Partial Reconfiguration
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

A Framework for Dynamically-Loaded Hardware Library (HLL) in FPGA Acceleration
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

A Hardware Framework for on-Chip FPGA Acceleration
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Design and Simulation of a Quaternary Memory Cell based on a Physical Memristor
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Dynamically-Loaded Hardware Libraries (HLL) Technology for Audio Applications
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

FPGA Acceleration by Dynamically-Loaded Hardware Libraries
Publication: Research › Report – Annual report year: 2016

Implementation of Hardware Accelerators on Zynq
Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction
Publication: Research - peer-review › Journal article – Annual report year: 2016

Performance/Power Space Exploration for Binary64 Division Units
Publication: Research - peer-review › Journal article – Annual report year: 2016

Characterization of RNS multiply-add units for power efficient DSP
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Power and thermal efficient numerical processing
Publication: Research - peer-review › Book chapter – Annual report year: 2015

Reliability in Warehouse-Scale Computing: Why Low Latency Matters
Nannarelli, A. 2015 Proceedings of MEDIAN Finale - Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale. p. 2-6
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Thermal Aware Floorplanning Incorporating Temperature Dependent Wire Delay Estimation
Publication: Research - peer-review › Journal article – Annual report year: 2015

Decimal Engine for Energy-Efficient Multicore Processors
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Energy Efficient FPGA based Hardware Accelerators for Financial Applications
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Guest Editors’ Introduction: Special Section on Computer Arithmetic
Publication: Research - peer-review › Journal article – Annual report year: 2014

Twenty Years of Research on RNS for DSP: Lessons Learned and Future Perspectives
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Layout-Driven Post-Placement Techniques for Temperature Reduction and Thermal Gradient Minimization
Publication: Research - peer-review › Journal article – Annual report year: 2013

Truncated multipliers through power-gating for degrading precision arithmetic
Comments on 'Improving the speed of decimal division'
Lang, T. & Nannarelli, A. 2012 In : I E T Computers and Digital Techniques. 6, 6, p. 370-371
Publication: Research - peer-review » Article in proceedings – Annual report year: 2012

Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications
Publication: Research - peer-review » Article in proceedings – Annual report year: 2012

Direct Measurement of Power Dissipated by Monte Carlo Simulations on CPU and FPGA Platforms
Publication: Research » Report – Annual report year: 2013

Imprecise Arithmetic for Low Power Image Processing
Publication: Research - peer-review » Article in proceedings – Annual report year: 2012

Power and Aging Characterization of Digital FIR Filters Architectures
Publication: Research - peer-review » Article in proceedings – Annual report year: 2012

Power Efficient Design of Parallel/Serial FIR Filters in RNS
Publication: Research - peer-review » Article in proceedings – Annual report year: 2012

Power Efficient Division and Square Root Unit
Publication: Research - peer-review » Journal article – Annual report year: 2012

Degrading Precision Arithmetics for Low-power FIR Implementation
Publication: Research - peer-review » Article in proceedings – Annual report year: 2011

FPGA Based Acceleration of Decimal Operations
Nannarelli, A. 2011 Proceedings of 2011 International Conference on ReConFigurable Computing and FPGA’s. IEEE, p. 146-151
Publication: Research - peer-review » Article in proceedings – Annual report year: 2011

FPGA Implementation of Decimal Processors for Hardware Acceleration
Publication: Research - peer-review » Article in proceedings – Annual report year: 2011

Power and Thermal Management of System-on-Chip
Publication: Research » Ph.D. thesis – Annual report year: 2011
Radix-16 Combined Division and Square Root Unit
Publication: Research - peer-review › Article in proceedings – Annual report year: 2011

Sloppy Addition and Multiplication
Publication: Research › Report – Annual report year: 2011

Temperature Dependent Wire Delay Estimation in Floorplanning
Publication: Research - peer-review › Article in proceedings – Annual report year: 2011

Modelling, Synthesis, and Configuration of Networks-on-Chips
Publication: Research › Ph.D. thesis – Annual report year: 2010

Degrading Precision Arithmetic for Low Power Signal Processing
Publication: Research - peer-review › Article in proceedings – Annual report year: 2010

Design of Large Polyphase Filters in the Quadratic Residue Number System
Publication: Research - peer-review › Article in proceedings – Annual report year: 2010

Low Power Hardware Platforms
Publication: Research › Book chapter – Annual report year: 2010

On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters
Publication: Research › Book chapter – Annual report year: 2010

Post-placement temperature reduction techniques
Publication: Research - peer-review › Article in proceedings – Annual report year: 2010

Power Dissipation Challenges In Multicore Floating-Point Units
Publication: Research - peer-review › Article in proceedings – Annual report year: 2010

Temperature Aware Power Optimization for Multicore Floating-Point Units
Publication: Research - peer-review › Article in proceedings – Annual report year: 2010

Division Unit for Binary Integer Decimals
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009
Fast Multi Operand Decimal Adders using Digit Compressors with Decimal Carry Generation
Publication: Research › Report – Annual report year: 2009

Hardware Implementation of Real-Time MPEG Analysis and Deblocking for Video Enhancement
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009

Multiple Constant Multiplication through Residue Number System
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009

Thermal Modeling Based on SPICE Simulation
Publication: Research - peer-review › Article in proceedings – Annual report year: 2009

ADAPTO: Full-Adder Based Reconfigurable Architecture for Bit Level Operations
Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Appendix to Power Dissipation in Division
Publication: Research › Report – Annual report year: 2008

A Variant of a Radix-10 Combinational Multiplier
Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Net Balanced Floorplanning Based on Elastic Energy Model
Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters
Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Power Dissipation in Division
Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Reducing Power Dissipation in Pipelined Accumulators
Publication: Research › Article in proceedings – Annual report year: 2008
A Radix-10 Digit-Recurrence Division Unit: Algorithm and Architecture
Lang, T. & Nannarelli, A. 2007 In : I E E E Transactions on Computers. 56, 6, p. 727-739
Publication: Research - peer-review › Journal article – Annual report year: 2007

Combined Radix-10 and Radix-16 Division Unit
Publication: Research - peer-review › Article in proceedings – Annual report year: 2007

Impact of RNS Coding Overhead on FIR Filters Performance
Publication: Research - peer-review › Article in proceedings – Annual report year: 2007

Low-power adaptive filter based on RNS components
Publication: Research - peer-review › Article in proceedings – Annual report year: 2007

Residue Number System for Low Power DSP Applications
Publication: Research - peer-review › Article in proceedings – Annual report year: 2007

A 1.5 GFLOPS Reciprocal Unit for Computer Graphics
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

A hybrid RNS adaptive filter for channel equalization
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

A Radix-10 Combinational Multiplier
Publication: Research - peer-review › Article in proceedings – Annual report year: 2006

Digit-Recurrence Dividers with Reduced Logical Depth
Publication: Research - peer-review › Journal article – Annual report year: 2005

Low Latency Digit-Recurrence Reciprocal and Square-Root Reciprocal Algorithm and Architecture
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

Low Power and Low Leakage Implementation of RNS FIR Filters
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005
Programmable Power-of-two RNS Scaler and its Application to a QRNS Polyphase Filter
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

A tool for automatic generation of RTL-level VHDL description of RNS FIR filters
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Low-power implementation of polyphase filters in Quadratic Residue Number System
Publication: Research - peer-review › Article in proceedings – Annual report year: 2004

Projects:

Time-predictable VLIW Processor
Abbaspour, S., Schoeberl, M., Sparsø, J., Nannarelli, A., Kirner, R. & Pedersen, R. U.
15/01/2012 → 09/12/2015
Project: PhD

Asynchronous Network-on-Chip for Time-Predictable Multi-Core Embedded Systems
Kasapaki, E., Sparsø, J., Schoeberl, M., Nannarelli, A., Jantsch, A. & Yakovlev, A.
01/10/2011 → 19/06/2015
Project: PhD

Optimized Networking for Energy Harvesting Wireless Sensor Networks
Fafoutis, X., Dragoni, N., Madsen, J., Nannarelli, A., Plosila, J. P. & Vain, J.
01/12/2010 → 26/05/2014
Project: PhD

System-Level Design to Support Early Design Stages and Evolvable Development of Embedded Systems
Gan, J., Pop, P., Madsen, J., Nannarelli, A., Curescu, C. & Popentiu, F.
15/12/2009 → 26/05/2014
Project: PhD

System-Level Design of Continuous Flow Microfluidic Biochips
15/09/2009 → 07/03/2013
Project: PhD

A Framework for Modeling, Simulation and Design Space Exploration of Digital Microfluidic Biochips
01/02/2008 → 31/08/2011
Project: PhD

Power and Thermal Management of System-on-chips
Liu, W., Nannarelli, A., Madsen, J., Pop, P., Alonso, D. A. & Tisserand, A.
15/10/2007 → 01/06/2011
Project: PhD

Network-on-chip: Applikationer og topologioptimering
Stuart, M. B., Sparsø, J., Nannarelli, A., Pop, P., Jantsch, A. & Pimentel, A. D.
01/10/2006 → 30/06/2010
System-Level Design Methodologies for Platform-based Multiprocessor SoC Designs
Virk, K. M., Madsen, J., Nannarelli, A., Jerraya, A. A. & Nurmi, J. A.
01/06/2004 → 05/11/2008
Project: PhD

Intra-Chip Communication
Bjerregaard, T., Sparsø, J., Nannarelli, A., Ginosar, R. & Goossens, K.
01/09/2002 → 10/02/2006
Project: PhD

High-Level Synthesis of Asynchronous
Nielsen, S. F., Sparse, J., Madsen, J., Nannarelli, A., Lavagno, L. & Peeters, A.
01/08/2001 → 06/06/2005
Project: PhD