Face Recognition using Approximate Arithmetic
Research output: Research › Report – Annual report year: 2018

Handwritten Digit Classification using 8-bit Floating Point based Convolutional Neural Networks
Research output: Research › Report – Annual report year: 2018

Tunable Floating-Point for Embedded Machine Learning Algorithms Implementation
Research output: Research - peer-review › Article in proceedings – Annual report year: 2018

Tunable Floating-Point for Energy Efficient Accelerators
Research output: Research - peer-review › Article in proceedings – Annual report year: 2018

A Multi-Format Floating-Point Multiplier for Power-Efficient Operations
Research output: Research - peer-review › Article in proceedings – Annual report year: 2017

Digital Arithmetic: Division Algorithms
Research output: Research - peer-review › Book chapter – Annual report year: 2017

RNS Applications in Digital Signal Processing
Research output: Research - peer-review › Book chapter – Annual report year: 2017

Robust Throughput Boosting for Low Latency Dynamic Partial Reconfiguration
Research output: Research - peer-review › Article in proceedings – Annual report year: 2017

A Framework for Dynamically-Loaded Hardware Library (HLL) in FPGA Acceleration
Research output: Research - peer-review › Article in proceedings – Annual report year: 2016
Decimal Engine for Energy-Efficient Multicore Processors
Research output: Research - peer-review › Article in proceedings – Annual report year: 2014

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Research output: Research - peer-review › Article in proceedings – Annual report year: 2014

Guest Editors’ Introduction: Special Section on Computer Arithmetic
Research output: Research - peer-review › Journal article – Annual report year: 2014

Twenty Years of Research on RNS for DSP: Lessons Learned and Future Perspectives
Research output: Research - peer-review › Article in proceedings – Annual report year: 2014

Layout-Driven Post-Placement Techniques for Temperature Reduction and Thermal Gradient Minimization
Research output: Research - peer-review › Article in proceedings – Annual report year: 2013

Truncated multipliers through power-gating for degrading precision arithmetic
Research output: Research - peer-review › Article in proceedings – Annual report year: 2014

Comments on 'Improving the speed of decimal division'
Lang, T. & Nannarelli, A. 2012 In : I E T Computers and Digital Techniques. 6, 6, p. 370-371
Research output: Research - peer-review › Comment/debate – Annual report year: 2012

Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications
Research output: Research - peer-review › Article in proceedings – Annual report year: 2012

Direct Measurement of Power Dissipated by Monte Carlo Simulations on CPU and FPGA Platforms
Research output: Research › Report – Annual report year: 2013

Imprecise Arithmetic for Low Power Image Processing
Research output: Research - peer-review › Article in proceedings – Annual report year: 2012

Power and Aging Characterization of Digital FIR Filters Architectures
Research output: Research - peer-review › Article in proceedings – Annual report year: 2012

Power Efficient Design of Parallel/Serial FIR Filters in RNS
Research output: Research - peer-review › Article in proceedings – Annual report year: 2012
**Power Efficient Division and Square Root Unit**
Research output: Research - peer-review › Journal article – Annual report year: 2012

**Degrading Precision Arithmetics for Low-power FIR Implementation**
Research output: Research - peer-review › Article in proceedings – Annual report year: 2011

**FPGA Based Acceleration of Decimal Operations**
Research output: Research - peer-review › Article in proceedings – Annual report year: 2011

**FPGA Implementation of Decimal Processors for Hardware Acceleration**
Research output: Research - peer-review › Article in proceedings – Annual report year: 2011

**Power and Thermal Management of System-on-Chip**
Research output: Research › Ph.D. thesis – Annual report year: 2011

**Radix-16 Combined Division and Square Root Unit**
Research output: Research - peer-review › Article in proceedings – Annual report year: 2011

**Sloppy Addition and Multiplication**
Research output: Research › Report – Annual report year: 2011

**Temperature Dependent Wire Delay Estimation in Floorplanning**
Research output: Research - peer-review › Article in proceedings – Annual report year: 2011

**Modelling, Synthesis, and Configuration of Networks-on-Chips**
Research output: Research › Ph.D. thesis – Annual report year: 2010

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**Design of Large Polyphase Filters in the Quadratic Residue Number System**
Research output: Research - peer-review › Article in proceedings – Annual report year: 2010

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On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters
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287 p.
Research output: Research › Book chapter – Annual report year: 2010

Post-placement temperature reduction techniques
Research output: Research - peer-review › Article in proceedings – Annual report year: 2010

Power Dissipation Challenges in Multicore Floating-Point Units
Research output: Research - peer-review › Article in proceedings – Annual report year: 2010

Temperature Aware Power Optimization for Multicore Floating-Point Units
Research output: Research - peer-review › Article in proceedings – Annual report year: 2010

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Research output: Research - peer-review › Article in proceedings – Annual report year: 2009

Fast Multi Operand Decimal Adders using Digit Compressors with Decimal Carry Generation
Research output: Research › Report – Annual report year: 2009

Hardware Implementation of Real-Time MPEG Analysis and Deblocking for Video Enhancement
Research output: Research - peer-review › Article in proceedings – Annual report year: 2009

Multiple Constant Multiplication through Residue Number System
Research output: Research - peer-review › Article in proceedings – Annual report year: 2009

Thermal Modeling Based on SPICE Simulation
Research output: Research - peer-review › Article in proceedings – Annual report year: 2009

ADAPTO: Full-Adder Based Reconfigurable Architecture for Bit Level Operations
Research output: Research - peer-review › Article in proceedings – Annual report year: 2008

Appendix to Power Dissipation in Division
Research output: Research › Report – Annual report year: 2008
A Variant of a Radix-10 Combinational Multiplier
Research output: Research - peer-review › Article in proceedings – Annual report year: 2008

Net Balanced Floorplanning Based on Elastic Energy Model
Research output: Research - peer-review › Article in proceedings – Annual report year: 2008

On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters
Research output: Research - peer-review › Article in proceedings – Annual report year: 2008

Power Dissipation in Division
Research output: Research - peer-review › Article in proceedings – Annual report year: 2008

Reducing Power Dissipation in Pipelined Accumulators
Research output: Research - peer-review › Article in proceedings – Annual report year: 2008

Residue Number Systems: a Survey
Research output: Research › Report – Annual report year: 2008

A Radix-10 Digit-Recurrence Division Unit: Algorithm and Architecture
Research output: Research - peer-review › Journal article – Annual report year: 2007

Combined Radix-10 and Radix-16 Division Unit
Research output: Research - peer-review › Article in proceedings – Annual report year: 2007

Impact of RNS Coding Overhead on FIR Filters Performance
Research output: Research - peer-review › Article in proceedings – Annual report year: 2007

Low-power adaptive filter based on RNS components
Research output: Research - peer-review › Article in proceedings – Annual report year: 2007

Residue Number System for Low Power DSP Applications
Research output: Research - peer-review › Article in proceedings – Annual report year: 2007

A 1.5 GFLOPS Reciprocal Unit for Computer Graphics
Research output: Research - peer-review › Article in proceedings – Annual report year: 2006
A hybrid RNS adaptive filter for channel equalization
Research output: Research - peer-review › Article in proceedings – Annual report year: 2006

A Radix-10 Combinational Multiplier
Research output: Research - peer-review › Article in proceedings – Annual report year: 2006

Digit-Recurrence Dividers with Reduced Logical Depth
Research output: Research - peer-review › Journal article – Annual report year: 2005

Low Latency Digit-Recurrence Reciprocal and Square-Root Reciprocal Algorithm and Architecture
Research output: Research - peer-review › Article in proceedings – Annual report year: 2005

Low Power and Low Leakage Implementation of RNS FIR Filters
Research output: Research - peer-review › Article in proceedings – Annual report year: 2005

Programmable Power-of-two RNS Scaier and its Application to a QRNS Polyphase Filter
Research output: Research - peer-review › Article in proceedings – Annual report year: 2005

A tool for automatic generation of RTL-level VHDL description of RNS FIR filters
Research output: Research - peer-review › Article in proceedings – Annual report year: 2004

Low-power implementation of polyphase filters in Quadratic Residue Number System
Research output: Research - peer-review › Article in proceedings – Annual report year: 2004

Projects:

Compilation Techniques for Flow-based Microfluidic Biochips
Schneider, A. R., Pop, P., Madsen, J., Nannarelli, A., Chakrabarty, K. & Ho, T.
Grundforskningsfonden
15/06/2015 → 15/08/2018
Project: PhD

System-Level Design Methodologies for Platform-based Multiprocessor SoC Designs
Virk, K. M., Madsen, J., Nannarelli, A., Jerraya, A. A. & Nurmi, J. A.
Offentlig finansiering
01/06/2004 → 05/11/2008
Project: PhD

System-Level Design of Continuous Flow Microfluidic Biochips
Forskningsrådsfinansiering
Network-on-chip: Applikationer og topologioptimering
Stuart, M. B., Sparsø, J., Nannarelli, A., Pop, P., Jantsch, A. & Pimentel, A. D.
DTU-lønnet stipendie
01/10/2006 → 30/06/2010
Project: PhD

Power and Thermal Management of System-on-chips
Liu, W., Nannarelli, A., Madsen, J., Pop, P., Alonso, D. A. & Tisserand, A.
DTU-lønnet stipendie
15/10/2007 → 01/06/2011
Project: PhD

Hi-Level Synthesis of Asynchronous
Nielsen, S. F., Sparsø, J., Madsen, J., Nannarelli, A., Lavagno, L. & Peeters, A.
DTU-lønnet stipendie
01/08/2001 → 06/06/2005
Project: PhD

Intra-Chip Communication
Bjerregaard, T., Sparsø, J., Nannarelli, A., Ginosar, R. & Goossens, S.
DTU-lønnet stipendie
01/09/2002 → 10/02/2006
Project: PhD

System-Level Design to Support Early Design Stages and Evolvable Development of Embedded Systems
Gan, J., Pop, P., Madsen, J., Nannarelli, A., Curescu, C. & Popentiu, F.
1/3 FUU, 1/3 inst 1/3 Andet
15/12/2009 → 26/05/2014
Project: PhD

Optimized Networking for Energy Harvesting Wireless Sensor Networks
Fafoutis, X., Dragoni, N., Madsen, J., Nannarelli, A., Plosila, J. P. & Vain, J.
Institut stipendie (DTU)
01/12/2010 → 26/05/2014
Project: PhD

Asynchronous Network-on-Chip for Time-Predictable Multi-Core Embedded Systems
Kasapaki, E., Sparsø, J., Schoeberl, M., Nannarelli, A., Jantsch, A. & Yakovlev, A.
Institut, samfinansiering
01/10/2011 → 19/06/2015
Project: PhD

Time-predictable VLIW Processor
Abbaspourseyedi, S., Schoeberl, M., Sparsø, J., Nannarelli, A., Kirner, R. & Pedersen, R. U.
Institut, samfinansiering
15/01/2012 → 09/12/2015
Project: PhD

A Framework for Modeling, Simulation ans Design Space Exploration of Digital Microfluidic Biochips
Institut stipendie (DTU)
01/02/2008 → 31/08/2011
Project: PhD