Alberto Nannarelli - DTU Orbit (13/01/2018)

Alberto Nannarelli

Organisations

Associate Professor, Department of Informatics and Mathematical Modeling
08/10/2003 → 07/04/2016 Former
an@imm.dtu.dk
VIP

Computer Science and Engineering
25/02/2012 → 18/02/2013 Former
VIP

Embedded Systems Engineering
25/02/2012 → 18/02/2013 Former
VIP

Organisations: Department of Applied Mathematics and Computer Science

Associate Professor, Department of Applied Mathematics and Computer Science
27/12/2012 → present
alna@dtu.dk
VIP

Embedded Systems Engineering
18/02/2013 → present
VIP

Publications:

A Multi-Format Floating-Point Multiplier for Power-Efficient Operations
In this work, we present a radix-16 multi-format multiplier to multiply 64-bit unsigned integer operands, double-precision and single-precision operands. The multiplier is sectioned in two lanes such that two single-precision multiplications can be computed in parallel. Radix-16 is chosen for the reduced number of partial products and the resulting power savings. The experimental results show that high power efficiency is obtained by issuing two single-precision multiplications per cycle. Moreover, by converting the double-precision numbers which fit to single-precision, further energy can be saved.

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Authors: Nannarelli, A. (Intern)
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Digital Arithmetic: Division Algorithms
Division is one of the basic arithmetic operations supported by every computer system. The operation can be performed and implemented by either hardware or software, or by a combination of the two. Although division is not as frequent as addition and multiplication, nowadays, most processors implement it in hardware to not compromise the overall computation performances. This entry explains the basic algorithms, suitable for hardware and software, to implement division in computer systems. Two classes of algorithms implement division or square root: digit-recurrence and multiplicative (e.g., Newton–Raphson) algorithms. The first class of algorithms, the digit-recurrence type, is particularly suitable for hardware implementation as it requires modest resources and provides good performance on contemporary technology. The second class of algorithms, the multiplicative type, requires significant hardware resources and is more suitable for software implementation on the existing multiply units. The purpose of this entry is to provide an introductory survey using a presentation style suitable for the interested non-specialist readers as well.
RNS Applications in Digital Signal Processing

In the past decades, the Residue Number System (RNS) has been adopted in DSP as an alternative to the traditional two's complement number system (TCS) because of the high speed of the obtained architectures and the savings in area and power dissipation. However, with the shrinking of device features and the advent of powerful design tools, the advantages offered by RNS are diminishing. In this chapter, we analyze the state-of-the-art RNS implementation for a number of common Digital Signal Processing (DSP) applications, we compare performance with respect to the TCS and consider trade-offs, and we identify some trends for implementing DSP on ASIC and FPGA platforms.

Robust Throughput Boosting for Low Latency Dynamic Partial Reconfiguration

Reducing the configuration time of portions of an FPGA at run time is crucial in contemporary FPGA-based accelerators. In this work, we propose a method to increase the throughput for FPGA dynamic partial reconfiguration by using standard IP blocks. The throughput is increased by over-clocking the configuration bitstream circuitry beyond the limits stated in the specifications of these standard blocks. The experimental results show that the most power efficient implementation can reach a throughput of about 780 MB/s, corresponding to a configuration latency of about 670 micro-seconds for bitstreams of 1.2 MB. We also investigate alternatives to boost the reconfiguration throughput and sketch a methodology to achieve the most power efficient implementation of FPGA-based accelerators.
A Framework for Dynamically-Loaded Hardware Library (HLL) in FPGA Acceleration

Hardware acceleration is often used to address the need for speed and computing power in embedded systems. FPGAs always represented a good solution for HW acceleration and, recently, new SoC platforms extended the flexibility of the FPGAs by combining on a single chip both high-performance CPUs and FPGA fabric.

The aim of this work is the implementation of hardware accelerators for these new SoCs. The innovative feature of these accelerators is the on-the-fly reconfiguration of the hardware to dynamically adapt the accelerator’s functionalities to the current CPU workload. The realization of the accelerators preliminarily requires also the profiling of both the SW (ARM CPU + NEON Units) and HW (FPGA) performance, an evaluation of the partial reconfiguration times and the development of an application-specific IP-cores library.

This paper focuses on the profiling aspect of both the SW and HW implementation of the same operations, using arithmetic routines (BLAS) as the reference point for benchmarking, and presents a comparison of the results in terms of speed, power consumption and resources utilization.

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A Hardware Framework for on-Chip FPGA Acceleration

In this work, we present a new framework to dynamically load hardware accelerators on reconfigurable platforms (FPGAs). Provided a library of application-specific processors, we load on-the-fly the specific processor in the FPGA, and we transfer the execution from the CPU to the FPGA-based accelerator. Results show that significant speed-up can be obtained by the proposed acceleration framework on system-on-chips where reconfigurable fabric is placed next to the CPUs. The speed-up is due to both the intrinsic acceleration in the application-specific processors, and to the increased parallelism.

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Design and Simulation of a Quaternary Memory Cell based on a Physical Memristor

Memristors were theorized more than fifty years ago, but only recently physical devices with memristor’s behavior have been fabricated and shipped. In this work, we experiment on one of these physical memristors by designing a memristor-based memory cell, implementing the cell, and testing it. Our experiments demonstrate that the memristor technology is not yet mature for practical applications, but, nevertheless, when production will provide reliable and dependable devices, memristor-based memory systems may replace CMOS memories with some advantages.

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Authors: Nannarelli, A. (Intern), Taylor, J. (Ekstern)
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Dynamically-Loaded Hardware Libraries (HLL) Technology for Audio Applications

In this work, we apply hardware acceleration to embedded systems running audio applications. We present a new framework, Dynamically-Loaded Hardware Libraries or HLL, to dynamically load hardware libraries on reconfigurable platforms (FPGAs). Provided a library of application-specific processors, we load on-the-fly the specific processor in the FPGA, and we transfer the execution from the CPU to the FPGA-based accelerator.

The proposed architecture provides excellent flexibility with respect to the different audio applications implemented, high quality audio, and an energy efficient solution.

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Authors: Esposito, A. (Ekstern), Lomuscio, A. (Ekstern), Nunzio, L. D. (Ekstern), Fazzolari, R. (Ekstern), Nannarelli, A. (Intern), Re, M. (Ekstern)
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FPGA Acceleration by Dynamically-Loaded Hardware Libraries

Hardware acceleration is a viable solution to obtain energy efficiency in data intensive computation.

In this work, we present a hardware framework to dynamically load hardware libraries, HLL, on reconfigurable platforms (FPGAs). Provided a library of application-specific processors, we load on-the-fly the specific processor in the FPGA, and we transfer the execution from the CPU to the FPGA-based accelerator.

Results show that significant speed-up and energy efficiency can be obtained by HLL acceleration on system-on-chips where reconfigurable fabric is placed next to the CPUs.

Implementation of Hardware Accelerators on Zynq

In the recent years it has become obvious that the performance of general purpose processors are having trouble meeting the requirements of high performance computing applications of today. This is partly due to the relatively high power consumption, compared to the performance, of general purpose processors, which has made hardware accelerators an essential part of several datacentres and the worlds fastest super-computers.

In this work, two different hardware accelerators were implemented on a Xilinx Zynq SoC platform mounted on the ZedBoard platform. The two accelerators are based on two different benchmarks, Monte Carlo simulation of European stock options and a Telco telephone billing application. Each of the accelerators test different aspects of the Zynq platform in terms of floating-point and binary coded decimal processing speed. The two accelerators are compared with the performance of the ARM Cortex-9 processor featured on the Zynq SoC, with regard to execution time, power dissipation and energy consumption.

The implementation of the hardware accelerators were successful. Use of the Monte Carlo processor resulted in a significant increase in performance. The Telco hardware accelerator showed a very high increase in performance over the ARM-processor.
Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction

In this paper, we describe an optimization for binary radix-16 (modified) Booth recoded multipliers to reduce the maximum height of the partial product columns to $\lceil n/4 \rceil$ for unsigned operands. This is in contrast to the conventional maximum height of $\lceil (n+1)/4 \rceil$. Therefore, a reduction of one unit in the maximum height is achieved. This reduction may add flexibility during the design of the pipelined multiplier to meet the design goals, it may allow further optimizations of the partial product array reduction stage in terms of area/delay/power and/or may allow additional addends to be included in the partial product array without increasing the delay. The method can be extended to Booth recoded radix-8 multipliers, signed multipliers, combined signed/unsigned multipliers, and other values of $n$. 

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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Santiago de Compostela, Politecnico di Torino
Authors: Antelo, E. (Ekstern), Montuschi, P. (Ekstern), Nannarelli, A. (Intern)
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Scopus rating (2013): SJR 1.315 SNIP 2.294 CiteScore 3.67
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 1.143 SNIP 2.072 CiteScore 3.16
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BFI (2011): BFI-level 1
Scopus rating (2011): SJR 1.029 SNIP 1.868 CiteScore 2.82
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 1
Performance/Power Space Exploration for Binary64 Division Units

The digit-recurrence division algorithm is used in several high-performance processors because it provides good tradeoffs in terms of latency, area and power dissipation. In this work we develop a minimally redundant radix-8 divider for binary64 (double-precision) aiming at obtaining better energy efficiency in the performance-per-watt space. The results show that the radix-8 divider, when compared to radix-4 and radix-16 units, requires less energy to complete a division for high clock rates.

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Web of Science (2016): Indexed yes
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Scopus rating (2015): SJR 0.708 SNIP 2.418 CiteScore 2.87
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Web of Science (2014): Indexed yes
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Scopus rating (2013): SJR 0.602 SNIP 2.406 CiteScore 2.46
ISI indexed (2013): ISI indexed yes
Web of Science (2013): Indexed yes
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Characterization of RNS multiply-add units for power efficient DSP

In the past decades, the Residue Number System (RNS) has been adopted in DSP as an alternative to the traditional two's complement number system (TCS) because of the savings in area, higher speed and reduced power dissipation. In this work, we perform a comprehensive Design Space Exploration (DSE) for a fused multiply-add unit by taking into account four metrics: area, delay, power consumption, and switching activity. The results of the DSE are verified against the TCS and RNS implementation of parallel FIR filters of different characteristics. In both the DSE and the filter implementation, we consider two design corners: maximum speed and minimum area. The experimental results demonstrate that for high data rates and high order filters, the RNS implementation is more power efficient than the TCS because of the reduced switching activity and the larger amount of low-power cells placed in the unit.

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Authors: Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Petricca, M. (Ekstern), Re, M. (Ekstern)
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Power and thermal efficient numerical processing
Numerical processing is at the core of applications in many areas ranging from scientific and engineering calculations to financial computing. These applications are usually executed on large servers or supercomputers to exploit their high speed, high level of parallelism and high bandwidth to memory.

Reliability in Warehouse-Scale Computing: Why Low Latency Matters
Warehouse sized buildings are nowadays hosting several types of large computing systems: from supercomputers to large clusters of servers to provide the infrastructure to the cloud. Although the main target, especially for high-performance computing, is still to achieve high throughput, the limiting factor of these warehouse-scale data centers is the power dissipation. Power is dissipated not only in the computation itself, but also in heat removal (fans, air conditioning, etc.) to keep the temperature of the devices within the operating ranges. The need to keep the temperature low within a minimal power envelope and to maintain high throughput and high reliability poses hard challenges.

In this work, we show that by moving part of the computation to accelerators, not only we reduce the latency of operations, but also make the system more energy efficient and reliable.

Thermal Aware Floorplanning Incorporating Temperature Dependent Wire Delay Estimation
Temperature has a negative impact on metal resistance and thus wire delay. In state-of-the-art VLSI circuits, large thermal gradients usually exist due to the uneven distribution of heat sources. The difference in wire temperature can lead to performance mismatch because wires of the same length can have different delay.

Traditional floorplanning algorithms use wirelength to estimate wire performance. In this work, we show that this does not
always produce a design with the shortest delay and we propose a floorplanning algorithm taking into account temperature
dependent wire delay as one metric in the evaluation of a floorplan. In addition, we consider other temperature dependent
factors such as congestion and interconnect reliability.

The experiment results show that a shorter delay can be achieved using the proposed method.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Knowles
Electronics, Oticon A/S, Arizona State University
Authors: Winther, A. (Ekstern), Liu, W. (Ekstern), Nannarelli, A. (Intern), Vrudhula, S. (Ekstern)
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- BFI (2016): BFI-level 1
- Scopus rating (2016): CiteScore 1.11 SJR 0.238 SNIP 0.864
- Web of Science (2016): Indexed yes
- BFI (2015): BFI-level 1
- Scopus rating (2015): SJR 0.26 SNIP 0.859 CiteScore 0.89
- Web of Science (2015): Indexed yes
- BFI (2014): BFI-level 1
- Scopus rating (2014): SJR 0.241 SNIP 1.1 CiteScore 0.97
- BFI (2013): BFI-level 1
- Scopus rating (2013): SJR 0.231 SNIP 1.234 CiteScore 1.02
- ISI indexed (2013): ISI indexed yes
- Web of Science (2013): Indexed yes
- BFI (2012): BFI-level 1
- Scopus rating (2012): SJR 0.218 SNIP 0.818 CiteScore 0.94
- ISI indexed (2012): ISI indexed yes
- BFI (2011): BFI-level 1
- Scopus rating (2011): SJR 0.22 SNIP 0.847 CiteScore 0.99
- ISI indexed (2011): ISI indexed yes
- Web of Science (2011): Indexed yes
- BFI (2010): BFI-level 1
- Scopus rating (2010): SJR 0.276 SNIP 0.937
- BFI (2009): BFI-level 1
- Scopus rating (2009): SJR 0.241 SNIP 0.843
- BFI (2008): BFI-level 1
- Scopus rating (2008): SJR 0.262 SNIP 0.915
- Scopus rating (2007): SJR 0.35 SNIP 0.848
- Scopus rating (2006): SJR 0.332 SNIP 0.57
- Scopus rating (2005): SJR 0.18 SNIP 0.751
- Scopus rating (2004): SJR 0.229 SNIP 0.774
- Scopus rating (2003): SJR 0.274 SNIP 0.997
- Scopus rating (2002): SJR 0.253 SNIP 0.62
- Scopus rating (2001): SJR 0.241 SNIP 0.572
Decimal Engine for Energy-Efficient Multicore Processors

Prior work demonstrated the use of specialized processors, or accelerators, be energy-efficient for binary floatingpoint (BFP) division and square root, and for decimal floatingpoint (DFP) operations. In the dark silicon era, where not all the circuits on the die can be powered simultaneously, we propose a hybrid BFP/DFP engine to perform BFP division and DFP addition, multiplication and division. The main purpose of this engine is to offload the binary floating-point units for this type of operations and reduce the latency for decimal operations, and power and temperature for the whole die.

Energy Efficient FPGA based Hardware Accelerators for Financial Applications

Field Programmable Gate Arrays (FPGAs) based accelerators are very suitable to implement application-specific processors using uncommon operations or number systems. In this work, we design FPGA-based accelerators for two financial computations with different characteristics and we compare the accelerator performance and energy consumption to a software execution of the application. The experimental results show that significant speed-up and energy savings, can be obtained for large data sets by using the accelerator at expenses of a longer development time.
Guest Editors’ Introduction: Special Section on Computer Arithmetic

The articles in this special issue focus on current trends and developments in the field of computer arithmetic. This is a field that encompasses the definition and standardization of arithmetic system for computers. The field also deals with issues of hardware and software implementations and their subsequent testing and verification. Many practitioners of the field also focus on the art and science of using computer arithmetic to carry out scientific and engineering computations. Computer arithmetic is therefore an interdisciplinary field that draws upon mathematics, computer science and electrical engineering. Advances in this field span from being highly theoretical (for instance, new exotic number systems) to being highly practical (for instance, new floating-point units for microprocessors).

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Scopus rating (2014): SJR 0.656 SNIP 2.424 CiteScore 2.56
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Scopus rating (2013): SJR 0.602 SNIP 2.406 CiteScore 2.46
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Scopus rating (2011): SJR 0.733 SNIP 2.054 CiteScore 2.42
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.607 SNIP 1.933
BFI (2009): BFI-level 2
Scopus rating (2009): SJR 0.737 SNIP 2.16
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.951 SNIP 2.451
Twenty Years of Research on RNS for DSP: Lessons Learned and Future Perspectives

In this paper, we discuss a number of issues emerged from our twenty-year long experience in applying the Residue Number System (RNS) to DSP systems. In early days, RNS was mainly used to reach the maximum performance in speed. Today, RNS is also used to obtain power efficient (tradeoffs speed-power) and reliable systems (redundant RNS). Advances in microelectronics and CAD tools play an important role in favoring one technology over another, and a winning choice of the past may become at disadvantage today. In this paper, we address a number of factors influencing the choice of RNS as the winning solution. From technology platforms (ASIC and FPGA), to issue related to modern design tools, from cost of memory, to cost of wiring, from power dissipation to thermal issues. Moreover, we mention how RNS can be helpful in implementing reliable architectures (fault detection and correction) in future VLSI systems.

Layout-Driven Post-Placement Techniques for Temperature Reduction and Thermal Gradient Minimization

With the continuing scaling of CMOS technology, on-chip temperature and thermal-induced variations have become a major design concern. To effectively limit the high temperature in a chip equipped with a cost-effective cooling system, thermal specific approaches, besides low power techniques, are necessary at the chip design level. The high temperature in hotspots and large thermal gradients are caused by the high local power density and the nonuniform power dissipation across the chip. With the objective of reducing power density in hotspots, we propose two placement techniques that spread cells in hotspots over a larger area. Increasing the area occupied by the hotspot directly reduces its power density, leading to a reduction in peak temperature and thermal gradient. To minimize the introduced overhead in delay and dynamic power, we maintain the relative positions of the coupling cells in the new layout. We compare the proposed methods in terms of temperature reduction, timing, and area overhead to the baseline method, which enlarges the circuit...
area uniformly. The experimental results showed that our methods achieve a larger reduction in both peak temperature and thermal gradient than the baseline method. The baseline method, although reducing peak temperature in most cases, has little impact on thermal gradient.

**General information**

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Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Oticon A/S, Politecnico di Torino
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BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.598 SNIP 1.915 CiteScore 2.18
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.665 SNIP 1.853 CiteScore 2.27
ISI indexed (2013): ISI indexed yes
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BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.65 SNIP 1.513 CiteScore 1.88
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.784 SNIP 1.595 CiteScore 2.08
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.775 SNIP 1.441
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.878 SNIP 1.693
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.889 SNIP 1.614
Web of Science (2008): Indexed yes
Scopus rating (2007): SJR 0.861 SNIP 1.765
Scopus rating (2006): SJR 0.847 SNIP 1.968
Web of Science (2006): Indexed yes
Scopus rating (2005): SJR 1.096 SNIP 2.096
Scopus rating (2004): SJR 0.86 SNIP 1.868
Scopus rating (2003): SJR 1.695 SNIP 2.002
Scopus rating (2002): SJR 1.56 SNIP 2.094
Scopus rating (2001): SJR 1.139 SNIP 1.559
Scopus rating (2000): SJR 0.331 SNIP 1.859
Truncated multipliers through power-gating for degrading precision arithmetic

When reducing the power dissipation of resource constrained electronic systems is a priority, some precision can be traded-off for lower power consumption. In signal processing, it is possible to have an acceptable quality of the signal even introducing some errors. In this work, we apply power-gating to multipliers to obtain a programmable truncated multiplier. The method consists in disabling the least-significant columns of the multiplier by power-gating logic in the partial products generation and accumulation array.

Comments on ‘Improving the speed of decimal division’

For original article see Kaivani, et al., ibid, vol. 5, pp. 393-404 (2011). Lang and Nannarelli comment on the paper of Kaivani, et al., which reported a proposed unit ~46% faster than the unit from their study. Lang and Nannarelli show in this comment that the evaluation done by Kaivani, et al. is based on wrong assumptions and the results of the comparison are erroneous.
Design of Power Efficient FPGA based Hardware Accelerators for Financial Applications

Using Field Programmable Gate Arrays (FPGAs) to accelerate financial derivative calculations is becoming very common. In this work, we implement an FPGA-based specific processor for European option pricing using Monte Carlo simulations, and we compare its performance and power dissipation to the execution on a CPU. The experimental results show that impressive results, in terms of speed-up and energy savings, can be obtained by using FPGA-based accelerators at expenses of a longer development time.

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Direct Measurement of Power Dissipated by Monte Carlo Simulations on CPU and FPGA Platforms

In this technical report, we describe how power dissipation measurements on different computing platforms (a desktop computer and an FPGA board) are performed by using a Hall effect-based current sensor. The chosen application is a Monte Carlo simulation for European option pricing which is a popular algorithm used in financial computations. The Hall effect probe measurements complement the measurements performed on the core of the FPGA by a built-in Xilinx power monitoring system.

Imprecise Arithmetic for Low Power Image Processing

Sometimes reducing the precision of a numerical processor, by introducing errors, can lead to significant performance (delay, area and power dissipation) improvements without compromising the overall quality of the processing. In this work, we show how to perform the two basic operations, addition and multiplication, in an imprecise manner by simplifying the hardware implementation. With the proposed "sloppy" operations, we obtain a reduction in delay, area and power dissipation, and the error introduced is still acceptable for applications such as image processing.
Power and Aging Characterization of Digital FIR Filters Architectures

With technology scaling, newer metrics have been introduced, in addition to delay, area, and power dissipation, to characterize the behavior of digital systems. While dynamic and static power dissipation still remain the most serious concern at nanometer lengths (65nm and below), process-variation, temperature and aging induced variations pose new challenges in the fabrication of the next generation of ICs. This work presents a detailed power and aging characterization of digital FIR filters in an industrial 45nm CMOS technology, and a design space exploration of different filter architectures with respect to throughput, area, power dissipation and aging. The exploration is intended to provide new design guidelines when considering aging of components in power/performance tradeoffs.

Power Efficient Design of Parallel/Serial FIR Filters in RNS

It is well known that the Residue Number System (RNS) provides an efficient implementation of parallel FIR filters especially when the filter order and the dynamic range are high. The two main drawbacks of RNS, need of converters and coding overhead, make a serialized implementation of the FIR filter potentially disadvantageous with respect to filters implemented in the conventional number systems. In this work, we show a number of solutions which demonstrate that the power efficiency of RNS FIR filters implemented serially is maintained in ASIC technology, while in modern FPGA technology RNS implementations are less efficient.
Power Efficient Division and Square Root Unit

Although division and square root are not frequent operations, most processors implement them in hardware to not compromise the overall performance. Two classes of algorithms implement division or square root: digit-recurrence and multiplicative (e.g., Newton-Raphson) algorithms. Previous work shows that division and square root units based on the digit-recurrence algorithm offer the best tradeoff delay-area-power. Moreover, the two operations can be combined in a single unit. Here, we present a radix-16 combined division and square root unit obtained by overlapping two radix-4 stages. The proposed unit is compared to similar solutions based on the digit-recurrence algorithm and it is compared to a unit based on the multiplicative Newton-Raphson algorithm.
Degrading Precision Arithmetics for Low-power FIR Implementation

In this paper a review of different techniques used to implement highly optimized DSP systems is presented. The case of study is the implementation of parallel FIR filters aimed to applications characterized by high speed and high selectivity in frequency where at the same time low power dissipation is mandatory. After a review of the possible "standard" optimization techniques, the paper addresses aggressive methodologies where power and area savings are obtained by introducing the concept of "Degrading Precision Arithmetic" (DPA). Three different approaches are discussed: DPA-I, based on selective bit freezing, DPA-II, based on VDD voltage scaling, and DPA-III, based on power gating. Some theoretical and simulative analysis of the introduced arithmetic errors and some implementation results are shown. A discussion on the suitability of these methodologies on standard cell technologies and FPGAs is also addressed. In our experience, these techniques are well known in the scientific community, but they are not extensively known in the design community, and, consequently, they are scarcely utilized.

General information
State: Published
Organisations: Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, University of Roma 'Tor Vergata'
Authors: Albicocco, P. (Ekstern), Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Petricca, M. (Ekstern), Re, M. (Ekstern)
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FPGA Based Acceleration of Decimal Operations
Field Programmable Gate-Arrays (FPGAs) can efficiently implement application specific processors in nonconventional number systems, such as the decimal (Binary-Coded Decimal, or BCD) number system required for accounting accuracy in financial applications. The main purpose of this work is to show that applications requiring several decimal (BCD) operations can be accelerated by a processor implemented on a FPGA board connected to the computer by a standard bus. For the case of a telephone billing application, we demonstrate that even a basic implementation of the decimal processor on the FPGA, without an advanced input/output interface, can achieve a speed-up of about 10 over its execution on the CPU of the hosting computer.

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FPGA Implementation of Decimal Processors for Hardware Acceleration
Applications in non-conventional number systems can benefit from accelerators implemented on reconfigurable platforms, such as Field Programmable Gate-Arrays (FPGAs). In this paper, we show that applications requiring decimal operations, such as the ones necessary in accounting or financial transactions, can be accelerated by Application Specific Processors (ASPs) implemented on FPGAs. For the case of a telephone billing application, we demonstrate that by accelerating the program execution on a FPGA board connected to the computer by a standard bus, we obtain a significant speed-up over its execution on the CPU of the hosting computer.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, Technical University of Denmark
Authors: Borup, N. (Ekstern), Dindorp, J. (Ekstern), Nannarelli, A. (Intern)
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Power and Thermal Management of System-on-Chip

With greater integration of VLSI circuits, power consumption and power density have increased dramatically resulting in high chip temperatures and presenting a heat removal challenge. To effectively limit the high temperature inside a chip, thermal specific approaches, besides low power techniques, are necessary at the chip design level. In this work, we investigate the power and thermal management of System-on-Chips (SoCs). Thermal analysis is performed in a SPICE simulation approach based on the electrical-thermal analogy. We investigate the impact of inter-connects on heat distribution in the substrate and present a way to consider temperature dependent signal delay in global wires at early design stages. With the aim of reducing high local power density in hotspots, we propose two placement techniques to spread hot cells over a larger area. The proposed methods are compared in terms of temperature reduction, timing and area overhead to the general method, which enlarges the circuit area uniformly. A case study analyzes the design of Floating Point Units (FPU) from an energy and a thermal perspective. For the division operation, we compare different implementations and illustrate the impact of power efficient dividers on the energy consumption and thermal distribution within the FPU and the on-chip cache. We also characterize the temperature dependent static dissipation to evaluate the reduction in leakage obtained from the decrease in temperature.

Radix-16 Combined Division and Square Root Unit

Division and square root, based on the digit-recurrence algorithm, can be implemented in a combined unit. Several implementations of combined division/square root units have been presented mostly for radices 2 and 4. Here, we present a combined radix-16 unit obtained by overlapping two radix-4 result digit selection functions, as it is normally done for division only units. The latency of the unit is reduced by retiming and low power methods are applied as well. The proposed unit is compared to a radix-4 combined division/square root unit, and to a radix-16 unit, obtained by cascading two radix-4 stages, which is similar to the one implemented in a state-of-the-art processor.
**Sloppy Addition and Multiplication**

Sometimes reducing the precision of a numerical processor, by introducing errors, can lead to significant performance (delay, area and power dissipation) improvements without compromising the overall quality of the processing. In this work, we show how to perform the two basic operations, addition and multiplication, in an imprecise manner by simplifying the hardware implementation. With the proposed “sloppy” operations, we obtain a reduction in delay, area and power dissipation, and the error introduced is still acceptable for applications such as image processing.

**Temperature Dependent Wire Delay Estimation In Floorplanning**

Due to large variations in temperature in VLSI circuits and the linear relationship between metal resistance and temperature, the delay through wires of the same length can be different. Traditional thermal aware floorplanning algorithms use wirelength to estimate delay and routability. In this work, we show that using wirelength as the evaluation metric does not always produce a floorplan with the shortest delay. We propose a temperature dependent wire delay estimation method for thermal aware floorplanning algorithms, which takes into account the thermal effect on wire delay. The experiment results show that a shorter delay can be achieved using the proposed method. In addition, we also discuss the congestion and reliability issues as they are closely related to routing and temperature.

**Modelling, Synthesis, and Configuration of Networks-on-Chips**

This thesis presents three contributions in two different areas of network-on-chip and system-on-chip research: Application modelling and identifying and solving different optimization problems related to two specific network-on-chip architectures.
The contribution related to application modelling is an analytical method for deriving the worst-case traffic pattern caused by an application and the cache-coherence protocol in a cache-coherent shared-memory system. The contributions related to network-on-chip optimization problems consist of two parts: The development and evaluation of six heuristics for solving the network synthesis problem in the MANGO network-on-chip, and the identification and formalization of the ReNoC configuration problem together with three heuristics for solving it.

**General information**
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Organisations: Biomedical Engineering, Department of Electrical Engineering, Embedded Systems Engineering, Department of Informatics and Mathematical Modeling
Authors: Stuart, M. B. (Intern), Sparsø, J. (Intern), Nannarelli, A. (Intern)
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### Degraded Precision Arithmetic for Low Power Signal Processing

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Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, University of Roma 'Tor Vergata'
Authors: Petricca, M. (Ekstern), Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Re, M. (Ekstern), Albicocco, P. (Ekstern)
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### Design of Large Polyphase Filters in the Quadratic Residue Number System

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Authors: Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Oster, Y. (Ekstern), Petricca, M. (Ekstern), Re, M. (Ekstern)
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Low Power Hardware Platforms

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On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters

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Post-placement temperature reduction techniques

With technology scaled to deep submicron era, temperature and temperature gradient have emerged as important design criteria. We propose two post-placement techniques to reduce peak temperature by intelligently allocating whitespace in the hotspots. Both methods are fully compliant with commercial technologies, and can be easily integrated with state-of-the-art thermal-aware design flow. Experiments in a set of tests on circuits implemented in STM 65nm technologies show that our methods achieve better peak temperature reduction than directly increasing circuit's area.

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Authors: Liu, W. (Intern), Nannarelli, A. (Intern)
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Electronic versions: Liu.pdf
Power Dissipation Challenges in Multicore Floating-Point Units

With increased densities on chips and the growing popularity of multicore processors and general-purpose graphics processing units (GPGPUs) power dissipation and energy consumption pose a serious challenge in the design of system-on-chips (SoCs) and a rise in costs for heat removal. In this work, we analyze the impact of power dissipation in floating-point (FP) units and we consider different alternatives in the implementation of FP-division that lead to substantial energy savings. We compare the implementation of division in a Fused Multiply-Add (FMA) unit based on the Newton-Raphson approximation algorithm to the implementation in a dedicated digit-recurrence unit. The results show a significant reduction of energy in a typical scientific application when the division digit-recurrence unit is used. In addition, we model the thermal behavior of the considered FP-units.

Division Unit for Binary Integer Decimals

In this work, we present a radix-10 division unit that is based on the digit-recurrence algorithm and implements binary encodings (binary integer decimal or BID) for significands. Recent decimal division designs are all based on the binary coded decimal (BCD) encoding. We adapt the radix-10 digit-recurrence algorithm to BID representation and implement the division unit in standard cell technology. The implementation of the proposed BID division unit is compared to that of a BCD based unit implementing the same algorithm. The comparison shows that for normalized operands the BID unit has the same latency as the BCD unit and reduced area, but the normalization is more expensive when implemented in BID.
Fast Multi Operand Decimal Adders using Digit Compressors with Decimal Carry Generation

Hardware Implementation of Real-Time MPEG Analysis and Deblocking for Video Enhancement

Multiple Constant Multiplication through Residue Number System
Thermal Modeling Based on SPICE Simulation

General information
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Organisations: Embedded Systems Engineering, Department of Informatics and Mathematical Modeling, Politecnico di Torino
Authors: Liu, W. (Intern), Calimera, A. (Ekstern), Nannarelli, A. (Intern), Macii, E. (Ekstern), Poncino, M. (Ekstern)
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ADAPTO: Full-Adder Based Reconfigurable Architecture for Bit Level Operations

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Authors: Cardarilli, G. C. (Ekstern), Di Nunzio, L. (Ekstern), Nannarelli, A. (Intern), Re, M. (Ekstern)
Pages: 3434-3437
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Appendix to Power Dissipation in Division

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Authors: Liu, W. (Intern), Nannarelli, A. (Intern)
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A Variant of a Radix-10 Combinational Multiplier

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Organisations: System-on-Chip Hardware, Department of Informatics and Mathematical Modeling, Politecnico di Milano
Authors: Dadda, L. (Ekstern), Nannarelli, A. (Intern)
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Publication: Research - peer-review › Article in proceedings – Annual report year: 2008

Net Balanced Floorplanning Based on Elastic Energy Model

Floorplanning is becoming more and more important in VLSI design flows, especially for system-on-chip (SoC) designs where IP blocks dominate standard cells. Moreover, in deep sub-micron technologies, where process variations can introduce extra signal skew, it is desirable to have floorplans with balanced net delays to increase the safety margins of the design. In this paper, we investigate the properties of floorplanning based on the elastic energy model. The B*-tree, which is based on an ordered binary tree, is used for circuit representation and the elastic energy is used as the cost function. To evaluate how well a net is balanced, we introduced a new metric ‘unbalancing’. A more balanced net would have a smaller ‘unbalancing’ value. Experimental results show that our approach can not only meet fixed-outline constraints, but also achieve significant improvements in net balance for all the circuits in the MCNC benchmark.

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Main Research Area: Technical/natural sciences
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On the Comparison of Different Number Systems in the Implementation of Complex FIR Filters

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Organisations: System-on-Chip Hardware, Department of Informatics and Mathematical Modeling
Authors: Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Re, M. (Ekstern)
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Power Dissipation in Division
A few classes of algorithms to implement division in hardware have been used over the years: division by digit-recurrence, by reciprocal approximation by iterative methods and by polynomial approximation. Due to the differences in the algorithms, a comparison among their implementation in terms of performance and precision is sometimes hard to make. In this work, we use power dissipation and energy consumption as metrics to compare among those different classes of algorithms. There are no previous works in the literature presenting such a comparison.

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Reducing Power Dissipation in Pipelined Accumulators

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Organisations: Department of Informatics and Mathematical Modeling, System-on-Chip Hardware
A Radix-10 Digit-Recurrence Division Unit: Algorithm and Architecture

In this work, we present a radix-10 division unit that is based on the digit-recurrence algorithm. The previous decimal division designs do not include recent developments in the theory and practice of this type of algorithm, which were developed for radix-2^k dividers. In addition to the adaptation of these features, the radix-10 quotient digit is decomposed into a radix-2 digit and a radix-5 digit in such a way that only five and two times the divisor are required in the recurrence. Moreover, the most significant slice of the recurrence, which includes the selection function, is implemented in radix-2, avoiding the additional delay introduced by the radix-10 carry-save additions and allowing the balancing of the paths to reduce the cycle delay. The results of the implementation of the proposed radix-10 division unit show that its latency is close to that of radix-16 division units (comparable dynamic range of significant) and it has a shorter latency than a radix-10 unit based on the Newton-Raphson approximation.

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Authors: Lang, T. (Ekstern), Nannarelli, A. (Intern)
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Combined Radix-10 and Radix-16 Division Unit

In this work we extend a previously proposed digit-recurrence radix-10 division unit to be able to perform also radix-16 division. The extension is simplified by the fact that in the radix-10 implementation the quotient digit is decomposed into two parts and that this decomposition is also appropriate for the radix-16 case. Moreover, to reduce the latency in the radix-10 the most-significant portion of the datapath, including the selection function, has been implemented in radix-2, so that the modifications of that part to include radix-16 consists mainly in combining the two modules to obtain the selection constants. The rest of the modifications relate to the generation of multiples, to the carry-save adder, to the carry-propagate adder, and to the on-the-fly conversion and rounding. The implementation results show that the delay of an iteration is similar to that of the radix-10 case and that the area is about thirty percent larger.

General information
Impact of RNS Coding Overhead on FIR Filters Performance

In this paper a low-power implementation of an adaptive FIR filter is presented. The filter is designed to meet the constraints of channel equalization for fixed wireless communications that typically requires a large number of taps, but a serial updating of the filter coefficients, based on the least mean squares (LMS) algorithm, is allowed. Previous work showed that the use of the residue number system (RNS) for the variable FIR filter grants advantages both in area and power consumption. On the other hand, the use of a binary serial implementation of the adaptation algorithm eliminates the need for complex scaling circuits in RNS. The advantages in terms of area and speed of the presented filter, with respect to its two's complement counterpart, are evaluated for implementations in standard cells.

Residue Number System for Low Power DSP Applications

In this paper a low-power implementation of an adaptive FIR filter is presented. The filter is designed to meet the constraints of channel equalization for fixed wireless communications that typically requires a large number of taps, but a serial updating of the filter coefficients, based on the least mean squares (LMS) algorithm, is allowed. Previous work showed that the use of the residue number system (RNS) for the variable FIR filter grants advantages both in area and power consumption. On the other hand, the use of a binary serial implementation of the adaptation algorithm eliminates the need for complex scaling circuits in RNS. The advantages in terms of area and speed of the presented filter, with respect to its two's complement counterpart, are evaluated for implementations in standard cells.
A 1.5 GFLOPS Reciprocal Unit for Computer Graphics

The reciprocal operation 1/d is a frequent operation performed in graphics processors (GPUs). In this work, we present the design of a radix-16 reciprocal unit based on the algorithm combining the traditional digit-by-digit algorithm and the approximation of the reciprocal by one Newton-Raphson iteration. We design a fully pipelined single-precision unit to be used in GPUs. The results of the implementation show that the proposed unit can sustain a higher throughput than that of a unit implementing the normal Newton-Raphson approximation, and its area is smaller.

A hybrid RNS adaptive filter for channel equalization

In this work a hybrid Residue Number System (RNS) implementation of an adaptive FIR filter is presented. The used adaptation algorithm is the Least Mean Squares (LMS). The filter has been designed to meet the constraints of specific class of applications. In fact, it is suitable for applications requiring a large number of taps where a serial updating of the filter coefficients is feasible (channel equalization or echo cancellation). In the literature, it has been shown that the RNS implementation of FIR filters grants earnings in area ad power consumption due to the introduced arithmetic simplifications. Vice versa, the RNS implementation of the adaptation algorithm needs scaling circuits that are complex and expensive in RNS arithmetic. For this reason, a serial binary implementation of the adaptation algorithm is chosen. The advantages in terms of area and speed of the RNS adaptive filter with respect to the two’s complement one have been evaluated for a standard cells implementation.
A Radix-10 Combinational Multiplier
In this work, we present a combinational decimal multiply unit which can be pipelined to reach the desired throughput. With respect to previous implementations of decimal multiplication, the proposed unit is combinational (parallel) and not sequential, has a simpler recoding of the operands which reduces the number of partial product precomputations and uses counters to eliminate the need of the decimal equivalent of a 4:2 adder. The results of the implementation show that the combinational decimal multiplier offers a good compromise between latency and area when compared to other decimal multiply units and to binary double-precision multipliers.

Digit-Recurrence Dividers with Reduced Logical Depth
In this paper, we propose a class of division algorithms with the aim of reducing the delay of the selection of the quotient digit by introducing more concurrency and flexibility in its computation. From the proposed class of algorithms, we select one that moves part of the selection function out of the critical path, with a corresponding reduction in the critical path compared with existing alternatives: we present the algorithm and describe the architectures for radix 4 and for radix 16. For radix 16, we use the scheme of overlapping two radix-4 stages. In both cases, radix 4 and radix 16, we show that our algorithms allow the design of units with well-balanced critical paths with consequent decreases of the cycle times. Moreover, in the radix-16 case, we include some additional speculation techniques. To estimate the speedup, we used a rough timing model based on logical effort. For both radices, we estimate a speedup of about 25 percent with respect to previous implementations. In the radix-4 case, this is achieved by using roughly the same area, while, in the radix-16 case, the area is increased by about 30 percent. We verified our estimations by performing a synthesis of the radix-4 units.
The reciprocal and square-root reciprocal operations are important in several applications. For these operations, we present algorithms that combine a digit-by-digit module and one iteration of a quadratic-convergence approximation. The latter is implemented by a digit-recurrence, which uses the digits produced by the digit-by-digit part. In this way, both parts execute in an overlapped manner, so that the total number of cycles is about half of the number that would be required by the digit-by-digit part alone. Because of the approximation, correct rounding of the result cannot be obtained directly in all cases; we propose a variable-time implementation that produces the correctly rounded result with a small average overhead. Radix-4 implementations are described and have been synthesized. They achieve the same cycle time as the
standard digit-by-digit implementation, resulting in a speed-up of about 2 and, because of the approximation part, the area factor is also about 2. We also show a combined implementation for both operations that has essentially the same complexity as that for square-root reciprocal alone.

**General information**

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Authors: Antelo, E. (Ekstern), Lang, T. (Ekstern), Montuschi, P. (Ekstern), Nannarelli, A. (Intern)  
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reciprocal, arithmetic, square-root reciprocal  
DOIs:  
10.1109/ARITH.2005.29  
Source: orbit  
Source-ID: 185665  
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

**Low Power and Low Leakage Implementation of RNS FIR Filters**  
The CMOS technology scaling is leading to the integration of ever more complex systems on silicon. On the other hand, the shrinking of the devices and the reduction of the supply voltage have significantly increased the static power dissipation, that in power budgets of nanometer technologies, cannot be neglected any longer. In this work, we take advantage of the properties of the Residue Number System (RNS) to implement FIR filters with reduced static and dynamic power consumption. The results show that the RNS filters offer a reduction of 50% in static power dissipation and a total power reduction of 40% with respect to the corresponding conventional filters.

**General information**

State: Published  
Organisations: Department of Informatics and Mathematical Modeling  
Authors: Cardarilli, G. C. (Ekstern), Re, A. D. (Ekstern), Nannarelli, A. (Intern), Re, M. (Ekstern)  
Pages: 1620-1624  
Publication date: 2005

**Host publication information**

Title of host publication: Proceedings of 39th Asilomar Conference on Signals, Systems, and Computers  
Publisher: IEEE  
ISBN (Print): 1-4244-0131-3  
Main Research Area: Technical/natural sciences  
Conference: Asilomar Conference on Signals, Systems and Computers, 01/01/2005  
RNS, FIR filters, low-power  
DOIs:  
10.1109/ACSSC.2005.1600042  
Source: orbit  
Source-ID: 185679  
Publication: Research - peer-review › Article in proceedings – Annual report year: 2005

**Programmable Power-of-two RNS Scaler and its Application to a QRNS Polyphase Filter**  
The scaling operation, i.e. the division by a constant factor followed by rounding, is a commonly used technique for reducing the dynamic range in Digital Signal Processing (DSP) systems. Usually, the constant is a power of two, and the implementation of the scaling is reduced to a right shift. This basic operation is not easily implementable in the Residue Number System (RNS) due to its non positional nature. A number of different algorithms have been presented in the literature for the RNS scaling. In this paper, several RNS dynamic reduction techniques have been analyzed and the selected one is applied to a polyphase filter bank. A comparison of the filter bank scaled with RNS to binary and binary to RNS conversions, and the RNS scaled implementation is presented. A reduction of area and power consumption of about 30% for the scaling block is obtained.

**General information**

State: Published  
Organisations: Department of Informatics and Mathematical Modeling
A tool for automatic generation of RTL-level VHDL description of RNS FIR filters

Although digital filters based on the Residue Number System (RNS) show high performance and low power dissipation, RNS filters are not widely used in DSP systems, because of the complexity of the algorithms involved. We present a tool to design RNS FIR filters which hides the RNS algorithms to the designer, and generates a synthesizable VHDL description of the filter taking into account several design constraints such as: delay, area and energy.

Low-power implementation of polyphase filters in Quadratic Residue Number System

The aim of this work is the reduction of the power dissipated in digital filters, while maintaining the timing unchanged. A polyphase filter bank in the Quadratic Residue Number System (QRNS) has been implemented and then compared, in terms of performance, area, and power dissipation to the implementation of a polyphase filter bank in the traditional two's complement system (TCS). The resulting implementations, designed to have the same clock rates, show that the QRNS filter is smaller and consumes less power than the TCS one.
Projects:

**Time-predictable VLIW Processor**

Department of Applied Mathematics and Computer Science  
Period: 15/01/2012 → 09/12/2015  
Number of participants: 6  
Phd Student:  
Abbaspourseyedi, Sahar (Intern)  
Supervisor:  
Sparsø, Jens (Intern)  
Main Supervisor:  
Schoeberl, Martin (Intern)  
Examiner:  
Nannarelli, Alberto (Intern)  
Kirsehre, Raimund (Ekstern)  
Pedersen, Rasmus Ulslev (Intern)

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Institut, samfinansiering  
Project: PhD

**Asynchronous Network-on-Chip for Time-Predictable Multi-Core Embedded Systems**

Department of Applied Mathematics and Computer Science  
Period: 01/10/2011 → 19/06/2015  
Number of participants: 6  
Phd Student:  
Kasapaki, Evangelia (Intern)  
Supervisor:  
Schoeberl, Martin (Intern)  
Main Supervisor:  
Sparsø, Jens (Intern)  
Examiner:  
Nannarelli, Alberto (Intern)  
Jantsch, Axel (Ekstern)  
Yakovlev, Alexandre (Ekstern)

**Financing sources**  
Source: Internal funding (public)  
Name of research programme: Institut, samfinansiering  
Project: PhD

**Optimized Networking for Energy Harvesting Wireless Sensor Networks**

Department of Applied Mathematics and Computer Science  
Period: 01/12/2010 → 26/05/2014  
Number of participants: 6  
Phd Student:  
Fafoutis, Xenofon (Intern)  
Supervisor:  
Madsen, Jan (Intern)  
Main Supervisor:  
Dragoni, Nicola (Intern)
System-Level Design to Support Early Design Stages and Evolvable Development of Embedded Systems

Department of Applied Mathematics and Computer Science
Period: 15/12/2009 → 26/05/2014
Number of participants: 6
Phd Student:
Gan, Junhe (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Curescu, Calin (Ekstern)
Popentiu, Florin (Intern)

Financing sources
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU)
Project: PhD

System-Level Design of Continuous Flow Microfluidic Biochips

Department of Informatics and Mathematical Modeling
Period: 15/09/2009 → 07/03/2013
Number of participants: 6
Phd Student:
Minhass, Wajid Hassan (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Catthoor, Francky (Ekstern)
Chakrabarty, Krishnendu (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: 1/3 FUU, 1/3 inst 1/3 Andet
Project: PhD

A Framework for Modeling, Simulation and Design Space Exploration of Digital Microfluidic Biochips

Department of Informatics and Mathematical Modeling
Period: 01/02/2008 → 31/08/2011
Number of participants: 6
Phd Student:
Maftei, Elena (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Pop, Paul (Intern)

Examiner:
Nannarelli, Alberto (Intern)
Chakrabarty, Krishnendu (Ekstern)
Peng, Zebo (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: Institut stipendie (DTU)
Project: PhD

Power and Thermal Management of System-on-chips
Department of Informatics and Mathematical Modeling
Period: 15/10/2007 → 01/06/2011
Number of participants: 6
Phd Student:
Liu, Wei (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Nannarelli, Alberto (Intern)
Examiner:
Pop, Paul (Intern)
Alonso, David Atienza (Ekstern)
Tisserand, Arnaud (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

Network-on-chip: Applikationer og topologioptimering
Department of Informatics and Mathematical Modeling
Period: 01/10/2006 → 30/06/2010
Number of participants: 6
Phd Student:
Stuart, Matthias Bo (Intern)
Supervisor:
Nannarelli, Alberto (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Pop, Paul (Intern)
Jantsch, Axel (Ekstern)
Pimentel, Andrew David (Ekstern)

Financing sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

System-Level Design Methodologies for Platform-based Multiprocessor SoC Designs
Department of Informatics and Mathematical Modeling
Period: 01/06/2004 → 05/11/2008
Number of participants: 5
Phd Student:
Virk, Kashif Munir (Intern)
Main Supervisor:
Madsen, Jan (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Jerraya, Ahmed Amine (Ekstern)
Nurmi, Jari Antero (Ekstern)

Finance sources
Source: Internal funding (public)
Name of research programme: Offentlig finansiering
Project: PhD

Intra-Chip Communication
Department of Informatics and Mathematical Modeling
Period: 01/09/2002 → 10/02/2006
Number of participants: 5
Phd Student:
Bjerregaard, Tobias (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Ginosar, Ran (Ekstern)
Goossens, Kees (Ekstern)

Finance sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD

Hig-Level Synthesis of Asynchronous
Department of Informatics and Mathematical Modeling
Period: 01/08/2001 → 06/06/2005
Number of participants: 6
Phd Student:
Nielsen, Sune Fallgaard (Intern)
Supervisor:
Madsen, Jan (Intern)
Main Supervisor:
Sparsø, Jens (Intern)
Examiner:
Nannarelli, Alberto (Intern)
Lavagno, Luciano (Ekstern)
Peeters, Ad (Ekstern)

Finance sources
Source: Internal funding (public)
Name of research programme: DTU-lønnet stipendie
Project: PhD