Activity-based DEVS modeling

Use of model-driven approaches has been increasing to significantly benefit the process of building complex systems. Recently, an approach for specifying model behavior using UML activities has been devised to support the creation of DEVS models in a disciplined manner based on the model driven architecture and the UML concepts. In this paper, we further this work by grounding Activity-based DEVS modeling and developing a fully-fledged modeling engine to demonstrate applicability. We also detail the relevant aspects of the created metamodel in terms of modeling and simulation. A significant number of the artifacts of the UML 2.5 activities and actions, from the vantage point of DEVS behavioral modeling, is covered in details. Their semantics are discussed to the extent of time-accurate requirements for simulation. We characterize them in correspondence with the specification of the atomic model behavior. We demonstrate the approach with simple, yet expressive DEVS models.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Arizona State University
Authors: Alshareef, A. (Ekstern), Sarjoughian, H. S. (Ekstern), Zarrin, B. (Intern)
Number of pages: 16
Pages: 116-131
Publication date: 2018
Main Research Area: Technical/natural sciences

Publication information
Journal: Simulation Notes Europe
Volume: 82
ISSN (Print): 2305-9974
Ratings:
Web of Science (2018): Indexed yes
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 2.4
Scopus rating (2015): CiteScore 2.26
Scopus rating (2014): CiteScore 2.22
Scopus rating (2013): CiteScore 2.08
Scopus rating (2012): CiteScore 2.12
Scopus rating (2011): CiteScore 1.73
Web of Science (2007): Indexed yes
Web of Science (2006): Indexed yes
Original language: English
Activity modeling, Behavioral modeling, DEVS, GMF, Model Driven Development, UML
DOIs:
10.1016/j.simpat.2017.12.009
Source: FindIt
Source-ID: 2395116938
Publication: Research - peer-review › Journal article – Annual report year: 2018

A multicore processor for time-critical applications

This article presents T-CREST many-core architecture specially designed and optimized for time-critical systems. —Tulika Mitra, National University of Singapore —Jürgen Teich, Friedrich-Alexander-Universität Erlangen-Nürnberg —Lothar Thiele, ETH Zurich.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schoeberl, M. (Intern), Pezzarossa, L. (Intern), Sparsø, J. (Intern)
Pages: 38-47
Publication date: 2018
Main Research Area: Technical/natural sciences

Publication information
Journal: IEEE Design & Test
Volume: 35
Issue number: 2
ISSN (Print): 2168-2356
An Integrated Framework to Specify Domain-Specific Modeling Languages

In this paper, we propose an integrated framework that can be used by DSL designers to implement their desired graphical domain-specific languages. This framework relies on Microsoft DSL Tools, a meta-modeling framework to build graphical domain-specific languages, and an extension of ForSpec, a logic-based specification language. The drawback of MS DSL Tools is that it does not provide a formal and rigorous approach for semantics specifications. In this framework, we use Microsoft DSL Tools to define the metamodel and graphical notations of DSLs, and an extended version of ForSpec as a formal language to define their semantics. Integrating these technologies under the umbrella of Microsoft Visual Studio IDE allows DSL designers to utilize a single development environment for developing their desired domain-specific languages.

General information
State: Published
AntibIoTic: Protecting IoT Devices Against DDoS Attacks
The 2016 is remembered as the year that showed to the world how dangerous Distributed Denial of Service attacks can be. Gauge of the disruptiveness of DDoS attacks is the number of bots involved: the bigger the botnet, the more powerful the attack. This character, along with the increasing availability of connected and insecure IoT devices, makes DDoS and IoT the perfect pair for the malware industry. In this paper we present the main idea behind AntibIoTic, a palliative solution to prevent DDoS attacks perpetrated through IoT devices.

DDoS-Capable IoT Malwares: Comparative Analysis and Mirai Investigation
The Internet of Things (IoT) revolution has not only carried the astonishing promise to interconnect a whole generation of traditionally “dumb” devices, but also brought to the Internet the menace of billions of badly protected and easily hackable objects. Not surprisingly, this sudden flooding of fresh and insecure devices fueled older threats, such as Distributed Denial of Service (DDoS) attacks. In this paper, we first propose an updated and comprehensive taxonomy of DDoS attacks, together with a number of examples on how this classification maps to real-world attacks. Then, we outline the current situation of DDoS-enabled malwares in IoT networks, highlighting how recent data support our concerns about the growing in popularity of these malwares. Finally, we give a detailed analysis of the general framework and the operating principles of Mirai, the most disruptive DDoS-capable IoT malware seen so far.
Design of a time-predictable multicore processor: the T-CREST project

Real-time systems need to deliver results in time and often this timely production of a result needs to be guaranteed. Static timing analysis can be used to bound the worst-case execution time of tasks. However, this timing analysis is only possible if the processor architecture is analysis friendly. This paper presents the T-CREST processor, a real-time multicore processor developed to be time-predictable and an easy target for static worst-case execution time analysis. We present how to achieve time-predictability at all levels of the architecture, from the processor pipeline, via a network-on-chip, up to the memory controller. The main architectural feature to provide time predictability is to use static arbitration of shared resources in a time-division multiplexing way.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schoeberl, M. (Intern)
Pages: 909-12
Publication date: 2018

Host publication information
Title of host publication: Proceedings of 2018 Design, Automation & Test in Europe Conference & Exhibition (DATE)
Publisher: IEEE
ISBN (Print): 978-3-9819263-0-9
Main Research Area: Technical/natural sciences
Conference: 2018 Design, Automation & Test in Europe Conference & Exhibition, Dresden, Germany, 19/03/2018 - 19/03/2018
DOIs:
10.23919/DATE.2018.8342138
Source: FindIt
Source-ID: 2419630360
Publication: Research - peer-review › Article in proceedings – Annual report year: 2018
Double-Loop Health Technology: Enabling Socio-technical Design of Personal Health Technology in Clinical Practice

Personal health technology is rapidly emerging as a response to the challenges associated with significant increase in chronic noncommunicable diseases. The overall design paradigm behind most of these applications is to manually and automatically sample data from sensors and smartphones and use this to provide patients with an awareness of their illness and give recommendation for treatment, care, and healthy living. Few of these systems are, however, designed to be part of a complex socio-technical care and treatment processes in existing healthcare systems and clinical pathways. In this chapter, we present a case of designing personal health technology for mental health, which is integrated into hospital-based treatment. This system helps patients to manage their disease by tracking and correlation behavior and disease progression and provide feedback to them, while also deployed as part of a clinical outpatient treatment. Hence, clinicians are “in the loop” and can monitor and provide feedback to patients. The chapter outlines the case and discusses lessons learned from it with respect to the socio-technical design of personal health technologies to be embedded as part of clinical treatment.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering, IT University of Copenhagen
Authors: Bardram, J. E. (Intern), Frost, M. (Ekstern)
Pages: 167–186
Publication date: 2018

Host publication information
Title of host publication: Designing Healthcare That Works - A Sociotechnical Approach
ISBN (Print): 978-0-12-812583-0
Chapter: 10
Main Research Area: Technical/natural sciences
Double-loop, Mental health, MONARCA, Noncommunicable diseases, Personal health technology, Socio-technical design DOIs: 10.1016/B978-0-12-812583-0.00010-9
Publication: Research - peer-review › Book chapter – Annual report year: 2018

Face Recognition using Approximate Arithmetic
Face recognition is image processing technique which aims to identify human faces and found its use in various different fields for example in security. Throughout the years this field evolved and there are many approaches and many different algorithms which aim to make the face recognition as effective as possible. The use of different approaches such as neural networks and machine learning can lead to fast and efficient solutions however, these solutions are expensive in terms of hardware resources and power consumption. A possible solution to this problem can be use of approximate arithmetic. In many image processing applications the results do not need to be completely precise and use of the approximate arithmetic can lead to reduction in terms of delay, space and power consumption. In this paper we examine possible use of approximate arithmetic in face recognition using Eigenfaces algorithm.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering, Technical University of Denmark
Authors: Marso, K. (Ekstern), Nannarelli, A. (Intern)
Number of pages: 25
Publication date: 2018

Publication information
Publisher: DTU Compute
Original language: English
Series: DTU Compute Technical Report-2018
Volume: 02
Main Research Area: Technical/natural sciences
Electronic versions: tr18_02_Nannarelli_A.pdf
Publication: Research › Report – Annual report year: 2018

From Monolithic to Microservices An Experience Report from the Banking Domain
Microservices have seen their popularity blossoming with an explosion of concrete applications in real-life software. Several companies are currently involved in a major refactoring of their back-end systems in order to improve scalability. This article presents an experience report of a real-world case study, from the banking domain, in order to demonstrate
how scalability is positively affected by reimplementing a monolithic architecture into microservices. The case study is based on the FX Core system for converting from one currency to another. FX Core is a mission-critical system of Danske Bank, the largest bank in Denmark and one of the leading financial institutions in Northern Europe.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Vienna University of Technology, Danske Bank Group, IRST Fondazione Bruno Kessler, Innopolis University
Authors: Bucchiarone, A. (Ekstern), Dragoni, N. (Intern), Dustdar, S. (Ekstern), Larsen, S. T. (Ekstern), Mazzara, M. (Ekstern)
Pages: 50-55
Publication date: 2018
Main Research Area: Technical/natural sciences

Publication information
Journal: IEEE Transactions on Software Engineering
Volume: 35
Issue number: 3
ISSN (Print): 0098-5589
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 3.237 SJR 0.548
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 5.51 SJR 0.874 SNIP 3.643
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 1.094 SNIP 3.943 CiteScore 4.97
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 1.296 SNIP 3.755 CiteScore 4.62
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 1.262 SNIP 4.601 CiteScore 5.29
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 1.516 SNIP 4.528 CiteScore 5.32
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 1.45 SNIP 4.519 CiteScore 5.11
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 1.559 SNIP 4.945
BFI (2009): BFI-level 2
Scopus rating (2009): SJR 1.794 SNIP 4.97
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 1.644 SNIP 5.731
Scopus rating (2007): SJR 1.77 SNIP 4.976
Scopus rating (2006): SJR 1.388 SNIP 4.996
Scopus rating (2005): SJR 1.586 SNIP 4.219
Scopus rating (2004): SJR 1.336 SNIP 3.503
Scopus rating (2003): SJR 1.479 SNIP 3.115
Scopus rating (2002): SJR 1.405 SNIP 2.916
Scopus rating (2001): SJR 1.449 SNIP 3.324
Scopus rating (2000): SJR 1.482 SNIP 3.734
Web of Science (2000): Indexed yes
Scopus rating (1999): SJR 1.389 SNIP 3.677
Original language: English
DOIs:
Lipsi: Probably the Smallest Processor in the World

While research on high-performance processors is important, it is also interesting to explore processor architectures at the other end of the spectrum: tiny processor cores for auxiliary functions. While it is common to implement small circuits for such functions, such as a serial port, in dedicated hardware, usually as a state machine or a combination of communicating state machines, these functionalities may also be implemented by a small processor. In this paper, we present Lipsi, a very tiny processor to make it possible to implement classic finite state machine logic in software at a minimal cost.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schoeberl, M. (Intern)
Pages: 18-30
Publication date: 2018

Host publication information
Title of host publication: Architecture of Computing Systems
Volume: 10793
Publisher: Springer
ISBN (Print): 9783319776095
Series: Lecture Notes in Computer Science
Volume: 10793
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
DOIs:
10.1007/978-3-319-77610-1_2
Source: FindIt
Source-ID: 2398002603
Publication: Research - peer-review › Article in proceedings – Annual report year: 2018

Model-Based Systems Engineering for Life-Sciences Instrumentation Development

General information
State: Accepted/In press
Organisations: Department of Management Engineering, Engineering Systems, Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Patou, F. (Intern), Dimaki, M. (Intern), Maier, A. (Intern), Svendsen, W. E. (Intern), Madsen, J. (Intern)
Publication date: 2018
Main Research Area: Technical/natural sciences

Publication information
Journal: Systems Engineering
ISSN (Print): 1098-1241
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 0.612 SJR 0.285
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 1.67 SJR 0.494 SNIP 1.026
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.456 SNIP 1.655 CiteScore 1.58
One-way shared memory

Standard multicore processors use the shared main memory via the on-chip caches for communication between cores. However, this form of communication has two limitations: (1) it is hardly time-predictable and therefore not a good solution for real-time systems and (2) this single shared memory is a bottleneck in the system. This paper presents a communication architecture for time-predictable multicore systems where core-local memories are distributed on the chip.

A network-on-chip constantly copies data from a sender core-local memory to a receiver core-local memory. As this copying is performed in one direction we call this architecture a one-way shared memory. With the use of time-division multiplexing for the memory accesses and the network-on-chip routers we achieve a time-predictable solution where the communication latency and bandwidth can be bounded. An example architecture for a 3×3 core processor and 32-bit wide links and memory ports provides a cumulative bandwidth of 29 bytes per clock cycle. Furthermore, the evaluation shows that this architecture, due to its simplicity, is small compared to other network-on-chip solutions.
Paper-based sensors for rapid detection of virulence factor produced by Pseudomonas aeruginosa

Pyocyanin is a toxin produced by Pseudomonas aeruginosa. Here we describe a novel paper-based electrochemical sensor for pyocyanin detection, manufactured with a simple and inexpensive approach based on electrode printing on paper. The resulting sensors constitute an effective electrochemical method to quantify pyocyanin in bacterial cultures without the conventional time consuming pretreatment of the samples. The electrochemical properties of the paper-based sensors were evaluated by ferri/ferrocyanide as a redox mediator, and showed reliable sensing performance. The paper-based sensors readily allow for the determination of pyocyanin in bacterial cultures with high reproducibility, achieving a limit of detection of 95 nM and a sensitivity of 4.30 μA/μM in standard culture media. Compared to the similar commercial ceramic based sensors, it is a 2.3-fold enhanced performance. The simple in-house fabrication of sensors for pyocyanin quantification allows researchers to understand in vitro adaptation of P. aeruginosa infections via rapid screenings of bacterial cultures that otherwise are expensive and time-consuming.

General information
State: Published
Organisations: Department of Biotechnology and Biomedicine, Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Infection Microbiology, Novo Nordisk Foundation Center for Biosustainability, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Copenhagen Center for Health Technology, Roskilde University, University of Copenhagen
Number of pages: 9
Publication date: 2018
Main Research Area: Technical/natural sciences

Publication information
Journal: P L o S One
Volume: 13
Issue number: 3
Article number: e0194157
ISSN (Print): 1932-6203
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SJR 1.164 SNIP 1.111
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 3.11 SJR 1.236 SNIP 1.101
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 1.427 SNIP 1.136 CiteScore 3.32
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 1.559 SNIP 1.148 CiteScore 3.54
Web of Science (2014): Indexed yes
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 1.772 SNIP 1.153 CiteScore 3.94
ISI indexed (2013): ISI indexed yes
Web of Science (2013): Indexed yes
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 1.982 SNIP 1.156 CiteScore 4.15
ISI indexed (2012): ISI indexed yes
Web of Science (2012): Indexed yes
BFI (2011): BFI-level 1
Scopus rating (2011): SJR 2.425 SNIP 1.233 CiteScore 4.58
Patmos: a time-predictable microprocessor

Current processors provide high average-case performance, as they are optimized for general purpose computing. However, those optimizations often lead to a high worst-case execution time (WCET). WCET analysis tools model the architectural features that increase average-case performance. To keep analysis complexity manageable, those models need to abstract from implementation details. This abstraction further increases the WCET bound. This paper presents a way out of this dilemma: a processor designed for real-time systems. We design and optimize a processor, called Patmos, for low WCET bounds rather than for high average-case performance. Patmos is a dual-issue, statically scheduled RISC processor. A method cache serves as the cache for the instructions and a split cache organization simplifies the WCET analysis of the data cache. To fill the dual-issue pipeline with enough useful instructions, Patmos relies on a customized compiler. The compiler also plays a central role in optimizing the application for the WCET instead of average-case performance.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Vienna University of Technology
Authors: Schoeberl, M. (Intern), Puffitsch, W. (Intern), Hepp, S. (Ekstern), Huber, B. (Ekstern), Prokesch, D. (Ekstern)
Pages: 1-35
Publication date: 2018
Main Research Area: Technical/natural sciences

Publication information
Journal: Real-Time Systems
Volume: 54
Issue number: 2
ISSN (Print): 0922-6443
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 2.237 SJR 0.257
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 2.26 SJR 0.392 SNIP 1.703
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.407 SNIP 1.904 CiteScore 1.85
Web of Science (2015): Indexed yes
Reconfiguration of Computation and Communication Resources in Multi-Core Real-Time Embedded Systems

Reconfigurable computing allows application programmers to significantly increase the speed of software algorithms by implementing computationally demanding tasks in hardware while maintaining a certain degree of flexibility. This can be achieved by using FPGAs to implement hardware accelerators that can be reconfigured when no longer needed, enabling the re-use of the resources of the FPGAs to realise new functionalities. For multi-core platforms, reconfiguration can be extended to the infrastructure supporting intercore communication and used to dynamically modify the characteristics of the communication channels between the tasks that are affected by the reconfiguration. This thesis investigates the use of reconfiguration in the context of multicore real-time systems targeting embedded applications. We address the reconfiguration of both the computation and the communication resources of a multi-core platform. Our approach is to associate reconfiguration with operational mode changes where the system, during normal operation, changes a subset of the executing tasks to adapt its behaviour to new conditions. Reconfiguration is therefore used during a mode change to modify the real-time guaranteed services provided by the hardware platform to fit the requirements of the current mode. The reconfiguration of the computation resources consists of altering the hardware implementation of selected resources, such as accelerators, and it is achieved by using the dynamic partial reconfiguration feature offered by FPGAs. With regards to this, we also present a lightweight reconfiguration controller, named RT-ICAP, specially developed to supporttime predictable dynamic partial reconfiguration. There configuration of the communication resources consists of setting up and tearing down the end-to-end channels offered by the communication fabric between the cores of the platform. To support this, we present a new network on chip architecture, named Argo 2, that allows instantaneous and time-predictable reconfiguration of the communication channels. Our reconfiguration-capable architecture is prototyped using the existing time-predictable multi-processor platform T-CREST. The thesis also presents low-level reconfiguration time analysis for these architectures. The evaluation of the proposed approach and the developed architectures is carried out through simulations and experiments.
out using synthetic benchmarks and hardware accelerators generated by high-level synthesis tools. For the reconfiguration of computation resources, the results show that the use of accelerators in combination with dynamic partial reconfiguration leads to better utilisation of the FPGA resources and tighter worst-case execution time bounds than a pure software solution. Moreover, the results show that using a configurable solution delivers a worst-case performance comparable to that of a non-reconfigurable solution. For the reconfiguration of communication resources, the results show that the worst-case reconfiguration time ranges from hundreds to thousands of clock cycles, making our solution considerably faster than other functionally equivalent networks-on-chips. In addition to the evaluation based on synthetic benchmarks, we also present a proof-of-concept case study based on a multi-core audio digital signal-processing application that combines reconfiguration of both the computation and communication resources. The case study shows that the presented approaches for reconfiguration can be effectively used in a real-world application and can lead to a reduction of the overall hardware size and better use of the platform resources while maintaining comparable computation performance with respect to a non-reconfigurable approach.

General information
State: Submitted
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Pezzarossa, L. (Intern)
Number of pages: 143
Publication date: 2018

Publication information
Publisher: DTU Compute
Original language: English
Series: DTU Compute PHD-2018
Volume: 469
ISSN: 0909-3192
Main Research Area: Technical/natural sciences

Relations
Projects:
Reconfiguration of Computation and Communication Resources in Multi-Core Real-Time Embedded Systems
Publication: Research › Ph.D. thesis – Annual report year: 2018

Selected papers from the 2nd IEEE Nordic Circuits and Systems Conference (NorCAS), 2016.
This special issue includes selected papers from the 2nd IEEE Nordic Circuits and Systems Conference (NorCAS), held in Linköping, Sweden, October 24-25, 2016. The IEEE NorCAS conference is the main circuits and systems event of the Nordic and Baltic countries representing both academia and the electronics industry. The NorCAS conference emerged in 2015 from the merger of the Norchip conference held annually in different Nordic and Baltic countries since 1983, and the International Symposium on Systems on chip held annually in Tampere, Finland since 1999.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Sparsø, J. (Intern)
Pages: 38-39
Publication date: 2018
Conference: Nordic Circuits and Systems Conference (NORCAS): NORCHIP and International Symposium of System-on-Chip (SoC), Linköping, Sweden, 23/10/2017 - 23/10/2017
Main Research Area: Technical/natural sciences

Publication information
Journal: Microprocessors and Microsystems
Volume: 60
ISSN (Print): 0141-9331
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 0.771 SJR 0.24
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 1.11 SJR 0.225 SNIP 0.822
Towards Domain-specific Flow-based Languages

Due to the significant growth of the demand for data-intensive computing, in addition to the emergence of new parallel and distributed computing technologies, scientists and domain experts are leveraging languages specialized for their problem domain, i.e., domain-specific languages, to help them describe their problems and solutions, instead of using general purpose programming languages. The goal of these languages is to improve the productivity and efficiency of the development and simulation of concurrent scientific models and systems. Moreover, they help to expose parallelism and to specify the concurrency within a component or across different independent components. In this paper, we introduce the concept of domain-specific flow-based languages which allows domain experts to use flow-based languages adapted to a particular problem domain. Flow-based programming is used to support concurrency, while the domain-specific part of these languages is used to define atomic processes and domain-specific validation rules for composite processes. We propose a modeling language that can be used to develop such domain-specific languages. Since this language allows one to define other languages, we often refer to it as a meta-modeling language.

General information

State: Published
Authors: Zarrin, B. (Intern), Baumeister, H. (Intern), Sarjoughian, H. S. (Ekstern)
Pages: 319-325
Supporting smartphone-based behavioral activation: A simulation study

Behavioral activation has shown to be a simple yet effective therapy for depressive patients. The method relies on extensive collection of patient reported activity data on an hourly basis. We are currently in the process of designing a smartphone-based behavioral activation system for depressive disorders. However, it is an open question to what degree patients would use this approach given the high demand for user input. In order to investigate this question, we collected paper-based behavioral activation forms from 5 patients, covering in total 18 weeks, 115 days, and 1,614 hours of self-reported activity data. In this paper we present an analysis of this data and discuss the implications for the design of a smartphone-based system for behavioral activation.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Copenhagen
Authors: Bardram, J. E. (Intern), Rohani, D. A. (Intern), Tuxen, N. (Ekstern), Faurholt-Jepsen, M. (Ekstern), Kessing, L. V. (Ekstern)
Number of pages: 14
Pages: 830-843
Publication date: 11 Sep 2017

Improving performance of single-path code through a time-predictable memory hierarchy

Deriving the Worst-Case Execution Time (WCET) of a task is a challenging process, especially for processor architectures that use caches, out-of-order pipelines, and speculative execution. Despite existing contributions to WCET analysis for these complex architectures, there are open problems. The single-path code generation overcomes these problems by generating time-predictable code that has a single execution trace. However, the simplicity of this approach comes at the cost of longer execution times. This paper addresses performance improvements for single-path code. We propose a time-predictable memory hierarchy with a prefetcher that exploits the predictability of execution traces in single-path code to speed up code execution. The new memory hierarchy reduces both the cache-miss penalty time and the cache-miss rate on the instruction cache. The benefit of the approach is demonstrated through benchmarks that are executed on an FPGA implementation.

General information
State: Published
**Pin-count reduction for continuous flow microfluidic biochips**

Microfluidic biochips are replacing the conventional biochemical analyzers integrating the necessary functions on-chip. We are interested in flow-based biochips, where a continuous flow of liquid is manipulated using integrated microvalves, controlled from external pressure sources via off-chip control pins. Recent research has addressed the physical design of such biochips. However, such research has so far ignored the pin-count, which rises with the increase in the number of microvalves. Given a biochip architecture and a biochemical application, we propose an algorithm for reducing the number of control pins required to run the application. The proposed algorithm has been evaluated on several biochips, including the AquaFlux biochip from Microfluidic Innovations LLC.
Mental health issues affect a significant portion of the world's population and can result in debilitating and life-threatening outcomes. To address this increasingly pressing healthcare challenge, there is a need to research novel approaches for early detection and prevention. In particular, ubiquitous systems can play a central role in revealing and tracking clinically relevant behaviors, contexts, and symptoms. Further, such systems can passively detect relapse onset and enable the opportune delivery of effective intervention strategies. However, despite their clear potential, the uptake of ubiquitous technologies into clinical mental healthcare is rare, and a number of challenges still face the overall efficacy of such technology-based solutions. The goal of this workshop is to bring together researchers interested in identifying, articulating, and addressing such issues and opportunities. Following the success of last year's inaugural workshop, we aim to continue facilitating the UbiComp community in developing a holistic approach for sensing and intervention in the context of mental health.
A Controller for Dynamic Partial Reconfiguration in FPGA-Based Real-Time Systems

In real-time systems, the use of hardware accelerators can lead to a worst-case execution-time speed-up, to a simplification of its analysis, and to a reduction of its pessimism. When using FPGA technology, dynamic partial reconfiguration (DPR) can be used to minimize the area, by only loading those accelerators that are needed at any given point in time. The DPR controllers provided by the FPGA vendors satisfy a wide range of requirements and rely on software to manage the reconfiguration. This approach may lead to slow reconfiguration and unpredictable timing. This paper presents an open-source DPR controller specially developed for hard real-time systems and prototyped in connection with the open-source multi-core platform for real-time applications T-CREST. The controller enables a processor to perform reconfiguration in a time-predictable manner and supports different operating modes. The paper also presents a software tool for bitstream conversion, compression, and for reconfiguration time analysis. The DPR controller is evaluated in terms of hardware cost, operating frequency, speed, and bitstream compression ratio vs. reconfiguration time trade-off. A simple application example is also presented with the scope of showing the reconfiguration features of the controller.

Activity-Based Collaboration for Interactive Spaces

Activity-based computing (ABC) is a conceptual and technological framework for designing interactive systems that offers a better mapping between the activities people conduct and the digital entities they use. In ABC, rather than interacting directly with lower-level technical entities like files, folder, documents, etc., users are able to interact with ‘activities’ which encapsulate files and other low-level resources. In ABC an ‘activity’ can be shared between collaborating users and can be accessed on different devices. As such, ABC is a framework that suits the requirements of designing interactive spaces. This chapter provides an overview of ABC with a special focus on its support for collaboration (‘Activity Sharing’) and multiple devices (‘Activity Roaming’). These ABC concepts are illustrated as implemented in two different interactive spaces technologies; ReticularSpaces [1] and the eLabBench [2, 3]. The chapter discusses the benefits of activity-based collaboration support for these interactive spaces, while also discussing limitations and challenges to be addressed in further research.
A language-based approach to modelling and analysis of Twitter interactions

More than a personal microblogging site, Twitter has been transformed by common use to an information publishing venue, which public characters, media channels and common people daily rely on for, e.g., news reporting and consumption, marketing, and social messaging. The use of Twitter in a cooperative and interactive setting calls for the precise awareness of the dynamics regulating message spreading. In this paper, we describe Twitlang, a language for modelling the interactions among Twitter accounts. The associated operational semantics allows users to precisely determine the effects of their actions on Twitter, such as post, reply-to or delete tweets. The language is implemented in the form of a Maude interpreter, Twitlanger, which takes a language term as an input and explores the computations arising from the term. By combining the strength of Twitlanger and the Maude model checker, it is possible to automatically verify communication properties of Twitter accounts. We illustrate the benefits of our executable formalisation by means of an application scenario inspired from real life. While the scenario highlights the benefits of adopting Twitter for a cooperative use in the everyday life, our analysis shows that appropriate settings are essential for a proper usage of the platform, in respect of fulfilling those communication properties expected within collaborative and interactive contexts.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, IMT Institute for Advanced Studies Lucca, Istituto di Informatica e Telematica, University of Camerino
Authors: Maggi, A. (Ekstern), Petrocchi, M. (Ekstern), Spognardi, A. (Intern), Tiezzi, F. (Ekstern)
Pages: 67-91
Publication date: 2017
Main Research Area: Technical/natural sciences

Publication Information
Journal: Journal of Logical and Algebraic Methods in Programming
Volume: 87
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 0.959 SJR 0.325
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 0.88 SJR 0.346 SNIP 1.171
Scopus rating (2015): SJR 0.243 SNIP 1.121 CiteScore 0.55
Original language: English
Twitter interactions and communications, Formal semantics, Verification, Model checking
DOIs:
10.1016/j.jlamp.2016.11.003
Source: FindIt
Source-ID: 2349429651
Publication: Research - peer-review › Journal article – Annual report year: 2017

A Multi-Format Floating-Point Multiplier for Power-Efficient Operations

In this work, we present a radix-16 multi-format multiplier to multiply 64-bit unsigned integer operands, double-precision and single-precision operands. The multiplier is sectioned in two lanes such that two single-precision multiplications can be computed in parallel. Radix-16 is chosen for the reduced number of partial products and the resulting power savings. The experimental results show that high power efficiency is obtained by issuing two single-precision multiplications per cycle. Moreover, by converting the double-precision numbers which fit to single-precision, further energy can be saved
Analysis of DDoS-capable IoT malwares

The Internet of Things (IoT) revolution promises to make our lives easier by providing cheap and always connected smart embedded devices, which can interact on the Internet and create added values for human needs. But all that glitters is not gold. Indeed, the other side of the coin is that, from a security perspective, this IoT revolution represents a potential disaster. This plethora of IoT devices that flooded the market were very badly protected, thus an easy prey for several families of malwares that can enslave and incorporate them in very large botnets. This, eventually, brought back to the top Distributed Denial of Service (DDoS) attacks, making them more powerful and easier to achieve than ever. This paper aims at provide an up-to-date picture of DDoS attacks in the specific subject of the IoT, studying how these attacks work and considering the most common families in the IoT context, in terms of their nature and evolution through the years. It also explores the additional offensive capabilities that this arsenal of IoT malwares has available, to mine the security of Internet users and systems. We think that this up-to-date picture will be a valuable reference to the scientific community in order to take a first crucial step to tackle this urgent security issue.

An Introduction to Malware

These notes, intended for use in DTU course 02233 on Network Security, give a short introduction to the topic of malware. The most important types of malware are described, together with their basic principles of operation and dissemination, and defenses against malware are discussed.
A resource-efficient network interface supporting low latency reconfiguration of virtual circuits in time-division multiplexing networks-on-chip

This paper presents a resource-efficient time-division multiplexing network interface of a network-on-chip intended for use in a multicore platform for hard real-time systems. The network-on-chip provides virtual circuits to move data between core-local on-chip memories. In such a platform, a change of the application’s operating mode may require reconfiguration of virtual circuits that are setup by the network-on-chip. A unique feature of our network interface is the instantaneous reconfiguration between different time-division multiplexing schedules, containing sets of virtual circuits, without affecting virtual circuits that persist across the reconfiguration. The results show that the worst-case latency from triggering a reconfiguration until the new schedule is executing, is in the range of 300 clock cycles. Experiments show that new schedules can be transmitted from a single master to all slave nodes for a 16-core platform in between 500 and 3500 clock cycles. The results also show that the hardware cost for an FPGA implementation of our architecture is considerably smaller than other network-on-chips with similar reconfiguration functionalities, and that the worst-case time for a reconfiguration is smaller than that seen in functionally equivalent architectures.
A Shared Scratchpad Memory with Synchronization Support

Multicore processors usually communicate via shared memory, which is backed up by a shared level 2 cache and a cache coherence protocol. However, this solution is not a good fit for real-time systems, where we need to provide tight guarantees on execution and memory access times. In this paper, we propose a shared scratchpad memory as a time-predictable communication and synchronization structure, instead of the level 2 cache. The shared on-chip memory is accessed via a time division multiplexing arbiter, isolating the execution time of load and store instructions between processing cores. Furthermore, the arbiter supports an extended time slot where an atomic load and store instruction can be executed to implement synchronization primitives. In the evaluation we show that a shared scratchpad memory is an efficient communication structure for a small number of processors; in our setup, 9 cores. Furthermore, we evaluate the efficiency of the synchronization support for implementation of classic locks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Hansen, H. E. (Ekstern), Maroun, E. J. (Ekstern), Kristensen, A. T. (Ekstern), Schoeberl, M. (Intern), Marquart, J. (Ekstern)
Number of pages: 6
Publication date: 2017
A Study on Text-Score Disagreement in Online Reviews

In this paper, we focus on online reviews and employ artificial intelligence tools, taken from the cognitive computing field, to help understand the relationships between the textual part of the review and the assigned numerical score. We move from the intuitions that (1) a set of textual reviews expressing different sentiments may feature the same score (and vice-versa), and (2) detecting and analyzing the mismatches between the review content and the actual score may benefit both service providers and consumers, by highlighting specific factors of satisfaction (and dissatisfaction) in texts. To prove the intuitions, we adopt sentiment analysis techniques and we concentrate on hotel reviews, to find polarity mismatches therein. In particular, we first train a text classifier with a set of annotated hotel reviews, taken from the Booking website. Then, we analyze a large dataset, with around 160k hotel reviews collected from TripAdvisor, with the aim of detecting a polarity mismatch, indicating if the textual content of the review is in line, or not, with the associated score. Using well-established artificial intelligence techniques and analyzing in depth the reviews featuring a mismatch between the text polarity and the score, we find that—on a scale of five stars—those reviews ranked with middle scores include a mixture of positive and negative aspects. The approach proposed here, beside acting as a polarity detector, provides an effective selection of reviews on an initial very large dataset— that may allow both consumers and providers to focus directly on the review subset featuring a text/score disagreement, which conveniently convey to the user a summary of positive and negative features of the review target.

A systematic and practical method for selecting systems engineering tools

The complexity of many types of systems has grown considerably over the last decades. Using appropriate systems engineering tools therefore becomes increasingly important. Starting the tool selection process can be intimidating because organizations often only have a vague idea about what they need. The tremendous number of available tools makes it difficult to get an overview and identify the best choice. Selecting wrong tools due to inappropriate analysis can have severe impact on the success of the company. This paper presents a systematic method for selecting systems engineering tools based on thorough analyses of the actual needs and the available tools. Grouping needs into categories, allow us to obtain a comprehensive set of requirements for the tools. The entire model-based systems engineering discipline was categorized for a modeling tool case to enable development of a tool specification. Correlating...
requirements and tool capabilities, enables us to identify the best tool for single-tool scenarios or the best set of tools for multi-tool scenarios. In both scenarios, we use gap analysis to prevent selection of infeasible tools. We used the method to select a traceability tool that has been in successful operation since 2013 at GN Hearing. We further utilized the method to select a set of tools that we used on pilot cases at GN Hearing for modeling, simulating and formally verifying embedded systems.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Copenhagen Center for Health Technology
Authors: Munck, A. (Intern), Madsen, J. (Intern)
Number of pages: 8
Pages: 201-208
Publication date: 2017

**Host publication information**

Title of host publication: Proceedings of the Systems Conference (SysCon), 2017 Annual IEEE International
Publisher: IEEE
Main Research Area: Technical/natural sciences
Conference: 11th Annual IEEE International Systems Conference (SysCon) 2017, Montreal, Canada, 24/04/2017 - 24/04/2017
Intelligence
DOIs: 10.1109/SYSCON.2017.7934729
Source: FindIt
Source-ID: 2371000477
Publication: Research - peer-review › Article in proceedings – Annual report year: 2018

A taxonomy of distributed denial of service attacks

The Internet of Things revolution promises to make our lives much easier by providing us cheap and convenient smart devices, but all that glitters is not gold. This plethora of devices that flooded the market, generally poorly designed with respect to security aspects, brought back to the top Distributed Denial of Service (DDoS) attacks which are now even more powerful and easier to achieve than the past. Understanding how these attacks work, in all their different forms, represents a first crucial step to tackle this urgent issue. To this end, in this paper we propose a new up-to-date taxonomy and a comprehensive classification of current DDoS attacks.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Örebro University
Authors: De Donno, M. (Intern), Giaretta, A. (Ekstern), Dragoni, N. (Intern), Spognardi, A. (Intern)
Pages: 100-7
Publication date: 2017

**Host publication information**

Title of host publication: Proceedings of 2017 International Conference on Information Society (i-Society)
Publisher: IEEE
ISBN (Print): 978-1-908320/86/5
Main Research Area: Technical/natural sciences
Conference: 2017 International Conference on Information Society, Dublin, Ireland, 17/07/2017 - 17/07/2017
DOIs: 10.23919/i-Society.2017.8354681
Source: FindIt
Source-ID: 2434426965
Publication: Research - peer-review › Article in proceedings – Annual report year: 2018

A Top-down Approach to Genetic Circuit Synthesis and Optimized Technology Mapping

Genetic logic circuits are becoming popular as an emerging field of technology. They are composed of genetic parts of DNA and work inside a living cell to perform a dedicated boolean function triggered by the presence or absence of certain proteins or other species.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Best practice for caching of single-path code

Single-path code has some unique properties that make it interesting to explore different caching and prefetching alternatives for the stream of instructions. In this paper, we explore different cache organizations and how they perform with single-path code.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Vienna University of Technology
Authors: Schoeberl, M. (Intern), Cilku, B. (Ekstern), Prokesch, D. (Ekstern), Puschner, P. (Ekstern)
Number of pages: 12
Publication date: 2017
Main Research Area: Technical/natural sciences

Publication information
Journal: Open Access Series in Informatics
Volume: 57
ISSN (Print): 2190-6807
Ratings:
ISI indexed (2013): ISI indexed no
ISI indexed (2012): ISI indexed no
ISI indexed (2011): ISI indexed no
Original language: English
Method cache, Prefetching, Single-path code
Electronic versions:
OASIcs_WCET_2017_2.pdf
DOIs:
10.4230/OASIcs.WCET.2017.2
Source: FindIt
Source-ID: 2394653551
Publication: Research - peer-review › Journal article – Annual report year: 2017

Best Practice for Caching of Single-Path Code

Single-path code has some unique properties that make it interesting to explore different caching and prefetching alternatives for the stream of instructions. In this paper, we explore different cache organizations and how they perform with single-path code.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Vienna University of Technology
Authors: Schoeberl, M. (Intern), Cilku, B. (Ekstern), Prokesch, D. (Ekstern), Puschner, P. (Ekstern)
Number of pages: 10
Publication date: 2017

Host publication information
Title of host publication: Proceedings of 17th International Workshop on Worst-Case Execution Time Analysis
Publisher: Schloss Dagstuhl - Leibniz-Zentrum fuer Informatik GmbH
ISBN (Electronic): 978-3-95977-057-6
BFI conference series: Worst-Case Execution Time Analysis (5010559)
Forskningen vedrørende anvendelsen af 'big data' indenfor sundhed er kun lige begyndt, og kan på sigt blive en stor hjælp i forhold til at tilrettelægge en mere personlig og helhedsorienteret sundhedsindsats for multisyge. Personlig sundhedssteknologi, som kort præsenteres i dette kapitel, rummer et stor potentiale for at gennemføre 'big data' analyser for den enkelte person, det vil sige hvor N=1. Der er store teknologiske udfordringer i at få lavet teknologier og metoder til at indsamle og håndtere personlige data, som kan deles, på tværs på en standardiseret, forsvarlig, robust, sikker og ikke mindst anonym facon.

Can Real-Time Systems Benefit from Dynamic Partial Reconfiguration?
In real-time systems, a solution where hardware accelerators are used to implement computationally intensive tasks can be easier to analyze, in terms of worst-case execution time (WCET), than a pure software solution. However, when using FPGAs, the amount and the complexity of the hardware accelerators are limited by the resources available. Dynamic partial reconfiguration (DPR) of FPGAs can be used to overcome this limitation by replacing the accelerators that are only required for limited amounts of time with new ones. This paper investigates the potential benefits of using DPR to implement hardware accelerators in real-time systems and presents an experimental analysis of the trade-offs between hardware utilization and WCET increase due to the reconfiguration time overhead of DPR. We also investigate the trade-off between the use of multiple specialized accelerators combined with DPR instead of the use of a more general accelerator. The results show that, for computationally intensive tasks, the use of DPR can lead to a more efficient use of the FPGA, while maintaining comparable computational performance.
Can smartphone-based electronic markers discriminate between patients with bipolar disorder, healthy first-degree relatives and healthy control individuals

General information
State: Published
Organisations: Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Cognitive Systems, Center for Energy Resources Engineering, Embedded Systems Engineering
Authors: Stanislaus, S. (Ekstern), Faurholt-Jepsen, M. (Ekstern), Vinberg, M. (Ekstern), Winther, O. (Intern), Frost, M. G. (Intern), Bardram, J. E. (Intern), Kessing, L. (Ekstern)
Number of pages: 1
Pages: 128-128
Publication date: 2017
Conference: 19th Annual Conference of the International Society for Bipolar Disorders, Washington DC, United States, 04/05/2017 - 04/05/2017
Main Research Area: Technical/natural sciences

Publication information
Journal: Bipolar Disorders (English Edition, Online)
Volume: 19
ISSN (Print): 1399-5618
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SJR 1.355 SNIP 2.354
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 4.35 SJR 2.481 SNIP 1.325
Scopus rating (2015): SJR 2.558 SNIP 1.488 CiteScore 4.68
Web of Science (2015): Indexed yes
Scopus rating (2014): SJR 3.286 SNIP 1.732 CiteScore 4.94
Scopus rating (2013): SJR 2.618 SNIP 1.509 CiteScore 4.8
Scopus rating (2012): SJR 3.084 SNIP 1.753 CiteScore 5.42
Scopus rating (2011): SJR 2.743 SNIP 1.625 CiteScore 4.84
Scopus rating (2010): SJR 2.711 SNIP 1.474
Scopus rating (2009): SJR 3.041 SNIP 1.566
Scopus rating (2008): SJR 2.764 SNIP 1.218
Scopus rating (2007): SJR 2.834 SNIP 1.368
Scopus rating (2006): SJR 2.228 SNIP 1.328
Scopus rating (2005): SJR 2.283 SNIP 1.128
Scopus rating (2004): SJR 2.23 SNIP 1.262
Scopus rating (2003): SJR 2.197 SNIP 0.988
Scopus rating (2002): SJR 2.48 SNIP 0.836
Scopus rating (2001): SJR 0.789 SNIP 0.653
Scopus rating (2000): SJR 1.096 SNIP 0.91
Original language: English
Source: FindIt
Source-ID: 2372727252
Publication: Research - peer-review › Conference abstract in journal – Annual report year: 2017

Collaborative Affordances of Medical Records
This article proposes the concept of Collaborative Affordances to describe physical and digital properties (i.e., affordances) of an artifact, which affords coordination and collaboration in work. Collaborative Affordances build directly on
Gibson (1977)’s affordance concept and extends the work by Sellen and Harper (2003) on the affordances of physical paper. Sellen and Harper describe how the physical properties of paper affords easy reading, navigation, mark-up, and writing, but focuses, we argue, mainly on individual use of paper and digital technology. As an extension to this, Collaborative Affordances focusses on the properties of physical and digital artifacts that affords collaborative activities. We apply the concept of Collaborative Affordances to the study of paper-based and electronic patient records in hospitals and detail how they afford collaboration through four types of Collaborative Affordances; being portable across patient wards and the entire hospital, by providing collocated access, by providing a shared overview of medical data, and by giving clinicians ways to maintain mutual awareness. We then discuss how the concept of Collaborative Affordances can be used in the design of new technology by providing a design study of a ‘Hybrid Patient Record’ (HyPR), which is designed to seamlessly blend and integrate paper-based with electronic patient records.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Lancaster University
Authors: Bardram, J. E. (Intern), Houben, S. (Forskerdatabase)
Number of pages: 36
Publication date: 2017
Main Research Area: Technical/natural sciences

Publication information
Journal: Computer Supported Cooperative Work
ISSN (Print): 0925-9724
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 1.435 SJR 0.326
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 3.47 SJR 0.747 SNIP 2.24
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.913 SNIP 2.121 CiteScore 3.21
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.765 SNIP 2.022 CiteScore 1.82
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 0.641 SNIP 1.745 CiteScore 2.58
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.441 SNIP 1.244 CiteScore 1.76
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.575 SNIP 1.506 CiteScore 1.7
ISI indexed (2011): ISI indexed no
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.501 SNIP 1.116
BFI (2009): BFI-level 2
Scopus rating (2009): SJR 0.587 SNIP 1.666
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.807 SNIP 1.647
Scopus rating (2007): SJR 0.704 SNIP 2.157
Scopus rating (2006): SJR 0.921 SNIP 2.683
Web of Science (2006): Indexed yes
Scopus rating (2005): SJR 0.671 SNIP 2.748
Scopus rating (2004): SJR 0.427 SNIP 2.364
Scopus rating (2003): SJR 0.54 SNIP 2.377
Scopus rating (2002): SJR 0.47 SNIP 1.59
Co-Simulation of Cyber-Physical System with Distributed Embedded Control

Cyber-Physical Systems (CPS) are integrations of computation and physical processes, with distributed embedded computation units, connected by network, controlling and monitoring a physical plant. The development of physical components is essentially different from the object-oriented software of the computation units. A major challenge developing CPS, is the nonlinear interaction between the discrete domain of the computational units and the continuous domain of the physical process. Model based development of both discrete and continuous systems has significantly benefited from specialized modelling and simulation tools in each domain. However, to realize the full potential of CPS, the abstraction-level of models and simulation has to unify both computation and physical dynamics. A solution to this, is a so called co-simulation where the coupled problem is divided into sub-systems where each constituent model can be solved by its optimum tool/solver in a distributed manner. This enables domain expert to work in domain specific tools while being able to simulate the complete CPS in a holistic manner. This dissertation provides a solution for doing co-simulation of CPS with distributed embedded control. This research has been conducted in collaboration with MAN Diesel & Turbo (MD&T) using their CPS, consisting of a two-stroke low speed engine with a distributed engine control system, as case study. Adapting a distributed control system to enable co-simulation is not trivial. How the lower layers of the embedded system software has been adapted to enable a deterministic and temporally controlled simulation will be presented. This includes how multiple controllers are compiled to dynamic link libraries that can be executed in parallel by a main process. A method for controlling execution and time progression on each controller has been developed along with a scheduling and network communication solution. To enable co-simulation with tools for modelling physical dynamics, the Functional Mockup Interface (FMI) standard for co-simulation has been implemented in the control system simulation. The solutions presented are validated through a set co-simulation experiments using the MD&T engine control system and different physical dynamic modelling tools. During the research new applications and requirements to the co-simulation environment was discovered. In large organizations like MD&T, tools, platforms and architecture used by different departments often deviate, making co-simulation and model exchange difficult. In collaboration with the EU Horizon 2020 project; Integrated Tool-chain for the model based design of Cyber-Physical Systems (INTO-CPS), a distributed co-simulation was made possible, that was able to co-simulate sub-systems of any architecture (32/64bit) and platform (Windows/Linux). Furthermore, when developing safety critical CPS that include a Human Machine Interface (HMI), the human interaction and cognitive assessment is of great importance. However, it is often difficult to obtain quantitative and evidence based data on the human in the loop. With an extension to the co-simulation environment it is possible to connect the control system simulation with the HMI in a hybrid co-simulation. In the hybrid co-simulation scenarios requiring human interaction can be formulated and tracked. The collected data can be used for analyzing the system applicability and intuitiveness, insuring correct and secure operation of MD&T engines. Validation and verification on hardware and engine test-benches is a major part of the development cost at MD&T. With the possibility of simulating the complete distributed control system, engineers are able to verify more of the component design before moving to the hardware test-bench. Furthermore, by introducing co-simulation, engineers can investigate and validate the holistic system dynamics during development before moving to the Engine test-bench and do model sharing between departments, reducing redundant modelling efforts. This research provides a solution for doing co-simulation of CPS with distributed control and proves that co-simulation can improve the development process, by reducing the amount of design and test loops during the design phase, thereby reducing the overall verification and validation cost.
Digital Arithmetic: Division Algorithms

Division is one of the basic arithmetic operations supported by every computer system. The operation can be performed and implemented by either hardware or software, or by a combination of the two. Although division is not as frequent as addition and multiplication, nowadays, most processors implement it in hardware to not compromise the overall computation performances. This entry explains the basic algorithms, suitable for hardware and software, to implement division in computer systems. Two classes of algorithms implement division or square root: digit-recurrence and multiplicative (e.g., Newton–Raphson) algorithms. The first class of algorithms, the digit-recurrence type, is particularly suitable for hardware implementation as it requires modest resources and provides good performance on contemporary technology. The second class of algorithms, the multiplicative type, requires significant hardware resources and is more suitable for software implementation on the existing multiply units. The purpose of this entry is to provide an introductory survey using a presentation style suitable for the interested non-specialist readers as well.

Distributed co-simulation of embedded control software with exhaust gas recirculation water handling system using INTO-CPS

Engineering complex Cyber-Physical Systems, such as emission reduction control systems for large two-stroke engines, require advanced modelling of both the cyber and physical aspects. Different tools are specialised for each of these domains and a combination of tools validating different properties is often desirable. However, it is non-trivial to be able to combine such different models of different constituent elements. In order to reduce the need for expensive tests on the real system it is advantageous to be able to combine such heterogeneous models in a joint co-simulation in order to reduce the overall costs of validation. This paper demonstrates how this can be achieved for a commercial system developed by MAN Diesel & Turbo using a newly developed tool chain based on the Functional Mock-up Interface standard for co-simulation supporting different operating systems. The generality of the suggested approach also enables future scenarios incorporating constituent models supplied by sub-suppliers while protecting their Intellectual Property.
EEG source imaging assists decoding in a face recognition task

EEG based brain state decoding has numerous applications. State of the art decoding is based on processing of the multivariate sensor space signal, however evidence is mounting that EEG source reconstruction can assist decoding. EEG source imaging leads to high-dimensional representations and rather strong a priori information must be invoked. Recent work by Edelman et al. (2016) has demonstrated that introduction of a spatially focal source space representation can improve decoding of motor imagery. In this work we explore the generality of Edelman et al. hypothesis by considering decoding of face recognition. This task concerns the differentiation of brain responses to images of faces and scrambled faces and poses a rather difficult decoding problem at the single trial level. We implement the pipeline using spatially focused features and show that this approach is challenged and source imaging does not lead to an improved decoding. We design a distributed pipeline in which the classifier has access to brain wide features which in turn does lead to a 15% reduction in the error rate using source space features. Hence, our work presents supporting evidence for the hypothesis that source imaging improves decoding.

Fast architecture-level synthesis of fault-tolerant flow-based microfluidic biochips

Microfluidic-based lab-on-a-chips have emerged as a popular technology for implementation of different biochemical test protocols used in medical diagnostics. However, in the manufacturing process or during operation of such chips, some faults may occur that leads to damage of the chip, which in turn results in wastage of expensive reagent fluids. In order to make the chip fault-tolerant, the state-of-the-art technique adopts simulated annealing (SA) based approach to synthesize a fault-tolerant architecture. However, the SA method is time consuming and non-deterministic with over-simplified model that usually derive sub-optimal results. Thus, we propose a progressive optimization procedure for the synthesis of fault-tolerant flow-based microfluidic biochips. Simulation results demonstrate that proposed method is efficient compared to the state-of-the-art techniques and can provide effective solutions in 88% (on average) less CPU time compared to state-of-the-art technique over three benchmark bioprotocols.
Fault-Tolerant Topology and Routing Synthesis for IEEE Time-Sensitive Networking

Time-Sensitive Networking (TSN) is a set of IEEE standards that extend Ethernet for safety-critical and real-time applications. TSN is envisioned to be widely used in several application areas, from industrial automation to in-vehicle networking. A TSN network is composed of end systems interconnected by physical links and bridges (switches). The data in TSN is exchanged via streams. We address safety-critical real-time systems, and we consider that the streams use the Urgency-Based Scheduler (UBS) traffic-type, suitable for hard real-time traffic. We are interested in determining a fault-tolerant network topology, consisting of redundant physical links and bridges, the routing of each stream in the applications, such that the architecture cost is minimized, the applications are fault-tolerant (i.e., the critical streams have redundant disjoint routes), and the timing constraints of the applications are satisfied. We propose three approaches to solve this optimization problem: (1) a heuristic solution, (2) a Greedy Randomized Adaptive Search Procedure (GRASP) metaheuristic, and (3) a Constraint Programming-based model. The approaches are evaluated on several test cases, including a test case from General Motors Company.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, General Motors Company
Authors: Gavrilut, V. M. (Intern), Zarrin, B. (Intern), Pop, P. (Intern), Samii, S. (Ekstern)
Number of pages: 10
Publication date: 2017

Host publication information
Title of host publication: Proceedings of the 25th International Conference on Real-Time Networks and Systems
Publisher: Association for Computing Machinery
ISBN (Print): 978-1-4503-5286-4
Main Research Area: Technical/natural sciences
Conference: 25th International Conference on Real-Time Networks and Systems, Grenoble, France, 04/10/2017 - 04/10/2017
Safety-Critical Systems, TSN, Fault-Tolerant Architectures
Electronic versions:
rtns2017.pdf
DOIs:
10.1145/3139258.3139284
Source: PublicationPreSubmission
Source-ID: 140106677
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017
High-level synthesis for reduction of WCET in real-time systems

The increasing design complexity of systems-on-chip (SoCs) requires designers to work at higher levels of abstraction. High-level synthesis (HLS) is one approach towards this. It allows designers to synthesize hardware directly from code written in a high-level programming language and to more quickly explore alternative implementations by re-running the synthesis with different optimization parameters and pragmas. HLS is particularly interesting for FPGA circuits, where different hardware implementations can easily be loaded into the target device. Another perspective on HLS is performance. Compared to executing the high-level language code on a processor, HLS can be used to create hardware that accelerates critical parts of the code. When discussing performance in the context or real-time systems, it is the worst-case execution time (WCET) of a task that matters. WCET obviously benefits from hardware acceleration, but it may also benefit from a tighter bound on the WCET. This paper explores the use of and integration of accelerators generated using HLS into a time-predictable processor intended for real-time systems. The high-level design tool, Vivado HLS, is used to generate hardware accelerators from benchmark code, and the system using the generated hardware accelerators is evaluated against the WCET of the original code. The design evaluation is carried out using the Patmos processor from the open-source T-CREST platform and implemented on a Xilinx Artix 7 FPGA. The WCET speed-up achieved is between a factor of 5 and 70.

High Performance with Prescriptive Optimization and Debugging

Parallel programming is the dominant approach to achieve high performance in computing today. Correctly writing efficient and fast parallel programs is a big challenge mostly carried out by experts. We investigate optimization and debugging of parallel programs.

We argue that automatic parallelization and automatic vectorization is attractive as it transparently optimizes programs. The thesis contributes an improved dependence analysis for explicitly parallel programs. These improvements lead to
more loops being vectorized, on average we achieve a speedup of 1.46 over the existing dependence analysis and vectorizer in GCC.

Automatic optimizations often fail for theoretical and practical reasons. When they fail we argue that a hybrid approach can be effective. Using compiler feedback, we propose to use the programmer’s intuition and insight to achieve high performance. Compiler feedback enlightens the programmer why a given optimization was not applied, and suggest how to change the source code to make it more amenable to optimizations. We show how this can yield significant speedups and achieve 2.4 faster execution on a real industrial use case.

To aid in parallel debugging we propose the prescriptive debugging model, which is a user-guided model that allows the programmer to use his intuition to diagnose bugs in parallel programs. The model is scalable, yet capable enough, to be general-purpose. In our evaluation we demonstrate low run time overhead and logarithmic scalability. This enable the model to be used on extremely large parallel systems.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Formal Methods, Embedded Systems Engineering
Authors: Jensen, N. B. (Intern), Probst, C. W. (Intern), Karlsson, S. (Intern)
Number of pages: 204
Publication date: 2017

**Publication Information**

Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English

Series: DTU Compute PHD-2016
Number: 437
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions: phd437_Jensen_NB.pdf

**Relations**

Projects:
High Performance with Prescriptive Optimization and Debugging
Publication: Research › Ph.D. thesis – Annual report year: 2017

**Improving Loop Dependence Analysis**

Programmers can no longer depend on new processors to have significantly improved single-thread performance. Instead, gains have to come from other sources such as the compiler and its optimization passes. Advanced passes make use of information on the dependencies related to loops. We improve the quality of that information by reusing the information given by the programmer for parallelization. We have implemented a prototype based on GCC into which we also add a new optimization pass. Our approach improves the amount of correctly classified dependencies resulting in 46% average improvement in single-thread performance for kernel benchmarks compared to GCC 6.1.

**General information**

State: Published
Organisations: Formal Methods, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Jensen, N. B. (Intern), Karlsson, S. (Intern)
Number of pages: 24
Pages: 1-24
Publication date: 2017
Main Research Area: Technical/natural sciences

**Publication Information**

Journal: Acm Transactions on Architecture and Code Optimization
Volume: 14
Issue number: 3
ISSN (Print): 1544-3973
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 1.005 SJR 0.301
Logic analysis and verification of n-input genetic logic circuits

Nature is using genetic logic circuits to regulate the fundamental processes of life. These genetic logic circuits are triggered by a combination of external signals, such as chemicals, proteins, light, and temperature, to emit signals to control other gene expressions or metabolic pathways accordingly. As compared to electronic circuits, genetic circuits exhibit stochastic behavior and do not always behave as intended. Therefore, there is a growing interest in being able to analyze and verify the logical behavior of a genetic circuit model, prior to its physical implementation in a laboratory. In this paper, we present an approach to analyze and verify the Boolean logic of a genetic circuit from the data obtained through stochastic analog circuit simulations. The usefulness of this analysis is demonstrated through different case studies illustrating how our approach can be used to verify the expected behavior of an n-input genetic logic circuit.

Methods and Tools for the Analysis, Verification and Synthesis of Genetic Logic Circuits,

Synthetic biology has emerged as an important discipline in which engineers and biologists are working together to design new and useful biological systems composed of genetic circuits. The purpose of developing genetic circuits is to carry out desired logical functions inside a living cell. This usually requires simulating the mathematical models of these genetic circuits and perceiving whether or not the circuit behaves appropriately. Furthermore, synthetic biology utilizes the concepts from electronic design automation (EDA) of abstraction and automated construction to generate genetic circuits with the aim to reduce the in-vitro (wet-lab) experiments. To address this, several automated tools have been developed to
improve the process of genetic design automation (GDA) with different capabilities. This thesis attempts to contribute to the advancement of GDA tools by introducing capabilities which we believe that no other existing GDA tools support. First, we introduce a user-friendly simulation tool, called D-VASim, which allows user to perform virtual laboratory experimentation by dynamically interacting with the model during runtime. This dynamic interaction with the model gives user a feeling of being in the lab performing wet-lab experiments virtually. This tool allows users to perform both deterministic and stochastic simulations. Next, this dissertation introduces a methodology to perform timing analyses of genetic logic circuits, which allows user to analyze the threshold value and propagation delays of genetic logic circuits. In this thesis, it has been demonstrated, through in-silico experimentation, that the threshold value and propagation delay plays a vital role in the correct functioning of genetic circuit. It has also been shown how some circuit parameters effect these two important design characteristics. This thesis also introduces an automated approach to analyze the behavior of genetic logic circuits from the simulation data. With this capability, the boolean logic of complex genetic circuits can be analyzed and/or verified automatically. It is also shown in this thesis that the proposed approach is effective to determine the variation in the behavior of genetic circuits when the circuit’s parameters are changed. In addition, the thesis also attempts to propose a synthesis and technology mapping tool, called GeneTech, for genetic circuits. It allows users to construct a genetic circuit by only specifying its behavior in the form of boolean expression. For technology mapping, this tool uses a gates library developed by the collective efforts of the researchers at MIT and Boston universities. It is shown experimentally that the tool is able to provide all feasible solutions, containing different genetic components, to achieve the specified boolean behavior. Finally, it has been shown how D-VASim can be used along with other tools for useful purposes, like model checking. With respect to this, an experimental workflow is proposed for checking genetic circuits using the statistical model checking (SMC) utility of the Uppaal tool and the timing analysis capability of D-VASim. We further demonstrated how the reliability of a simulation can be improved by using the real parameter values. In this regard, the relationship between the simulation parameters and real parameters have been derived.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Baig, H. (Intern), Madsen, J. (Intern), Pop, P. (Intern)
Number of pages: 253
Publication date: 2017

**Publication information**

Original language: English
Series: DTU Compute PHD-2017
Volume: 456
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions:
phd456_Baig_H.pdf

**Relations**

Projects:
Methods and Tools for the Analysis, Verification and Synthesis of Genetic Logic Circuits,
Publication: Research › Ph.D. thesis – Annual report year: 2017

**Microservices: Yesterday, Today, and Tomorrow**

Microservices is an architectural style inspired by service-oriented computing that has recently started gaining popularity. Before presenting the current state of the art in the field, this chapter reviews the history of software architecture, the reasons that led to the diffusion of objects and services first, and microservices later. Finally, open problems and future challenges are introduced. This survey primarily addresses newcomers to the discipline, while offering an academic viewpoint on the topic. In addition, we investigate some practical issues and point out a few potential solutions.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Formal Methods, University of Southern Denmark, University of Bologna, Innopolis University
Authors: Dragoni, N. (Intern), Giallorenzo, S. (Ekstern), Lafuente, A. (Intern), Mazzara, M. (Ekstern), Montesi, F. (Ekstern), Mustafin, R. (Ekstern), Safina, L. (Ekstern)
Pages: 195-216
Publication date: 2017
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Present and Ulterior Software Engineering
Paper-Based Digital Microfluidic Chip for Multiple Electrochemical Assay Operated by a Wireless Portable Control System

The printing and modular fabrication of a paper-based active microfluidic lab on a chip implemented with electrochemical sensors (ECSs) is developed and integrated on a portable electrical control system. The electrodes of a chip plate for active electrowetting actuation of digital drops and an ECS for multiple analysis assays are fabricated by affordable printing techniques. For enhanced sensitivity of the sensor, the working electrode is modified through the electrochemical method, namely by reducing graphene with voltammetry and coating gold nanoparticles by amperometry. Detachable sensor and absorber modules are assembled modularly on an open chip plate, forming various novel hybridized open–closed chip formats. By varying the coupled or decoupled sensor modules, excellent detection of three diagnostic biological molecules is demonstrated (glucose, dopamine, and uric acid in human serum). With a newly designed portable power supply and wireless control system, the active paper-based chip platform can be utilized as an advanced point-of-care device for multiple assays in digital microfluidics.

Performance Improvements and Congestion Reduction for Routing-based Synthesis for Digital Microfluidic Biochips

Routing-based synthesis for digital microfluidic biochips yields faster assay execution times compared to module-based synthesis. We show that routing-based synthesis can lead to deadlocks and livelocks in specific cases, and that dynamically detecting them and adjusting the probabilities associated with different droplet movements can alleviate the situation. We also introduce methods to improve the efficiency of wash droplet routing during routing-based synthesis, and to support non-reconfigurable modules, such as integrated heaters and detectors. We obtain increases in success rates when dealing with resource-constrained chips and reductions in average assay execution time.
Digital microfluidic biochip (DMFB), Routing-based synthesis, Wash droplets
Real-Time Audio Processing on the T-CREST Multicore Platform

Multicore platforms are nowadays widely used for audio processing applications, due to the improvement of computational power that they provide. However, some of these systems are not optimized for temporally constrained environments, which often leads to an undesired increase in the latency of the audio signal. This paper presents a real-time multicore audio processing system based on the T-CREST platform. T-CREST is a time-predictable multicore processor for real-time embedded systems. Multiple audio effect tasks have been implemented, which can be connected together in different configurations forming sequential and parallel effect chains, and using a network-on-chip for intercommunication between processors. The evaluation of the system shows that real-time processing of multiple effect configurations is possible, and that the estimation and control of latency ensures real-time behavior.

Reducing the rate and duration of Re-admissions among patients with unipolar disorder and bipolar disorder using smartphone-based monitoring and treatment - the RADMIS trials: Study protocol for two randomized controlled trials

Background: Unipolar and bipolar disorder combined account for nearly half of all morbidity and mortality due to mental and substance use disorders, and burden society with the highest health care costs of all psychiatric and neurological disorders. Among these, costs due to psychiatric hospitalization are a major burden. Smartphones comprise an innovative and unique platform for the monitoring and treatment of depression and mania. No prior trial has investigated whether the use of a smartphone-based system can prevent re-admission among patients discharged from hospital. The present RADMIS trials aim to investigate whether using a smartphone-based monitoring and treatment system, including an integrated clinical feedback loop, reduces the rate and duration of re-admissions more than standard treatment in unipolar disorder and bipolar disorder. Methods: The RADMIS trials use a randomized controlled, single-blind, parallel-group design. Patients with unipolar disorder and patients with bipolar disorder are invited to participate in each trial when discharged from psychiatric hospitals in The Capital Region of Denmark following an affective episode and randomized to either (1) a smartphone-based monitoring system including (a) an integrated feedback loop between patients and clinicians and (b) context-aware cognitive behavioral therapy (CBT) modules (intervention group) or (2) standard treatment (control group) for a 6-month trial period. The trial started in May 2017. The outcomes are (1) number and duration of re-admissions (primary), (2) severity of depressive and manic (only for patients with bipolar disorder) symptoms; psychosocial functioning; number of affective episodes (secondary), and (3) perceived stress, quality of life, self-rated depressive symptoms, self-rated manic symptoms (only for patients with bipolar disorder), recovery, empowerment, adherence to medication, wellbeing, ruminations, worrying, and satisfaction (tertiary). A total of 400 patients (200 patients with unipolar disorder and 200 patients with bipolar disorder) will be included in the RADMIS trials. Discussion: If the smartphone-based monitoring system proves effective in reducing the rate and duration of readmissions, there will be basis for using a system of this kind in the treatment of unipolar and bipolar disorder in general and on a larger scale.
In the past decades, the Residue Number System (RNS) has been adopted in DSP as an alternative to the traditional two’s complement number system (TCS) because of the high speed of the obtained architectures and the savings in area and power dissipation. However, with the shrinking of device features and the advent of powerful design tools, the advantages offered by RNS are diminishing. In this chapter, we analyze the state-of-the-art RNS implementation for a
number of common Digital Signal Processing (DSP) applications, we compare performance with respect to the TCS and consider trade-offs, and we identify some trends for implementing DSP on ASIC and FPGA platforms.

**Robust Throughput Boosting for Low Latency Dynamic Partial Reconfiguration**

Reducing the configuration time of portions of an FPGA at run time is crucial in contemporary FPGA-based accelerators. In this work, we propose a method to increase the throughput for FPGA dynamic partial reconfiguration by using standard IP blocks. The throughput is increased by over-clocking the configuration bitstream circuitry beyond the limits stated in the specifications of these standard blocks. The experimental results show that the most power efficient implementation can reach a throughput of about 780 MB/s, corresponding to a configuration latency of about 670 micro-seconds for bitstreams of 1.2 MB. We also investigate alternatives to boost the reconfiguration throughput and sketch a methodology to achieve the most power efficient implementation of FPGA-based accelerators.

**Safe Cooperating Cyber-Physical Systems using Wireless Communication**

This paper presents an overview of the ECSEL project entitled –Safe Cooperating Cyber-Physical Systems using Wireless Communication‖ (SafeCOP), which runs during the period 2016–2019. SafeCOP targets safety-related Cooperating Cyber-Physical Systems (CO-CPS) characterised by use of wireless communication, multiple stakeholders, dynamic system definitions (openness), and unpredictable operating environments. SafeCOP will provide an approach to the safety assurance of CO-CPS, enabling thus their certification and development. The project will define a runtime manager architecture for runtime detection of abnormal behaviour, triggering if needed a safe degraded mode. SafeCOP will also develop methods and tools, which will be used to produce safety assurance evidence needed to certify cooperative functions. SafeCOP will extend current wireless technologies to ensure safe and secure cooperation, and also contribute
to new standards and regulations, by providing certification authorities and standardization committees with the scientifically validated solutions needed to craft effective standards extended to also address cooperation and system-of-systems issues. The project has 28 partners from 6 European countries, and a budget of about 11 million Euros corresponding to about 1,300 person-months.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Alten Sverige AB, Mälardalen University
Authors: Pop, P. (Intern), Scholle, D. (Ekstern), Sljivo, I. (Ekstern), Hansson, H. (Ekstern), Widforss, G. (Ekstern), Rosqvist, M. (Ekstern)
Pages: 42-50
Publication date: 2017
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Microprocessors and Microsystems
Volume: 53
ISSN (Print): 0141-9331
Ratings:
  - BFI (2018): BFI-level 1
  - Web of Science (2018): Indexed yes
  - BFI (2017): BFI-level 1
  - Scopus rating (2017): SNIP 0.771 SJR 0.24
  - Web of Science (2017): Indexed Yes
  - BFI (2016): BFI-level 1
  - Scopus rating (2016): CiteScore 1.11 SJR 0.225 SNIP 0.822
  - Web of Science (2016): Indexed yes
  - BFI (2015): BFI-level 1
  - Scopus rating (2015): SJR 0.25 SNIP 0.857 CiteScore 0.89
  - Web of Science (2015): Indexed yes
  - BFI (2014): BFI-level 1
  - Scopus rating (2014): SJR 0.236 SNIP 1.057 CiteScore 0.97
  - BFI (2013): BFI-level 1
  - Scopus rating (2013): SJR 0.225 SNIP 1.182 CiteScore 1.02
  - ISI indexed (2013): ISI indexed yes
  - Web of Science (2013): Indexed yes
  - BFI (2012): BFI-level 1
  - Scopus rating (2012): SJR 0.214 SNIP 0.729 CiteScore 0.94
  - ISI indexed (2012): ISI indexed yes
  - BFI (2011): BFI-level 1
  - Scopus rating (2011): SJR 0.214 SNIP 0.797 CiteScore 0.99
  - ISI indexed (2011): ISI indexed yes
  - Web of Science (2011): Indexed yes
  - BFI (2010): BFI-level 1
  - Scopus rating (2010): SJR 0.255 SNIP 0.913
  - BFI (2009): BFI-level 1
  - Scopus rating (2009): SJR 0.223 SNIP 0.804
  - BFI (2008): BFI-level 1
  - Scopus rating (2008): SJR 0.256 SNIP 0.885
  - Scopus rating (2007): SJR 0.327 SNIP 0.841
  - Scopus rating (2006): SJR 0.372 SNIP 0.548
  - Scopus rating (2005): SJR 0.171 SNIP 0.671
  - Scopus rating (2004): SJR 0.208 SNIP 0.744
  - Scopus rating (2003): SJR 0.238 SNIP 0.99
  - Scopus rating (2002): SJR 0.227 SNIP 0.659
  - Scopus rating (2001): SJR 0.205 SNIP 0.536
Scheduling and Fluid Routing for Flow-Based Microfluidic Laboratories-on-a-Chip

Microfluidic laboratories-on-chip (LoCs) are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. There are several types of LoCs, each having its advantages and limitations. In this paper we are interested in flow-based LoCs, in which a continuous flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, switches, mixers and multiplexers, can be built. We consider that the architecture of the LoC is given, and we are interested in synthesizing an implementation, consisting of the binding of operations in the application to the functional units of the architecture, the scheduling of operations and the routing and scheduling of the fluid flows, such that the application completion time is minimized. To solve this problem, we propose a List Scheduling-based Application Mapping (LSAM) framework and evaluate it by using real-life as well as synthetic benchmarks. When biochemical applications contain fluids that may adsorb on the substrate on which they are transported, the solution is to use rinsing operations for contamination avoidance. Hence, we also propose a rinsing heuristic, which has been integrated in the LSAM framework.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of California at Riverside
Authors: Minhass, W. H. (Intern), McDaniel, J. (Ekstern), Raagaard, M. L. (Intern), Brisk, P. (Ekstern), Pop, P. (Intern), Madsen, J. (Intern)
Pages: 615 - 628
Publication date: 2017
Main Research Area: Technical/natural sciences
Security And Privacy Issues in Healthcare Monitoring Systems: A Case Study

Security and privacy issues are rarely taken into account in automated systems for monitoring elderly people in their home, exposing inhabitants to a number of threats they are usually not aware of. As a case study to expose the major vulnerabilities these systems are exposed to, this paper reviews a generic example of automated healthcare monitoring system. The security and privacy issues identified in this case study can be easily generalised and regarded as alarm bells for all the pervasive healthcare professionals.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Copenhagen Center for Health Technology, Embedded Systems Engineering, Technical University of Denmark
Authors: Handler, D. T. (Ekstern), Hauge, L. (Ekstern), Spognardi, A. (Intern), Dragoni, N. (Intern)
Pages: 383-388
Publication date: 2017

Host publication information
Title of host publication: Proceedings of the 10th International Joint Conference on Biomedical Engineering Systems and Technologies
Volume: 5
Publisher: SCITEPRESS Digital Library
ISBN (Print): 9789897582134
BFI conference series: International Joint Conference on Biomedical Engineering Systems and Technologies (5010258)
Main Research Area: Technical/natural sciences
Conference: 10th International Joint Conference on Biomedical Engineering Systems and Technologies, Porto, Portugal, 21/02/2017 - 21/02/2017
Security flows in OAuth 2.0 framework: A case study

The burst in smartphone use, handy design in laptops and tablets as well as other smart products, like cars with the ability to drive you around, manifests the exponential growth of network usage and the demand of accessing remote data on a large variety of services. However, users notoriously struggle to maintain distinct accounts for every single service that they use. The solution to this problem is the use of a Single Sign On (SSO) framework, with a unified single account to authenticate user’s identity throughout the different services. In April 2007, AOL introduced OpenAuth framework. After several revisions and despite its wide adoption, OpenAuth 2.0 has still several flaws that need to be fixed in several implementations. In this paper, we present a thorough review about both benefits of this single token authentication mechanism and its open flaws.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Argyriou, M. (Ekstern), Dragoni, N. (Intern), Spognardi, A. (Intern)
Pages: 396-406
Publication date: 2017

Host publication information
Publisher: Springer
ISBN (Print): 9783319662831
Series: Lecture Notes in Computer Science
Volume: 10489
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
Theoretical Computer Science, Computer Science (all), Computer Science, Logics and Meanings of Programs, Programming Languages, Compilers, Interpreters, Software Engineering, Systems and Data Security, Computer Applications, Computer Systems Organization and Communication Networks
DOIs:
10.1007/978-3-319-66284-8_33
Source: FindIt
Source-ID: 2390613130
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

Simulation Approach for Timing Analysis of Genetic Logic Circuits

Constructing genetic logic circuits is an application of synthetic biology in which parts of the DNA of a living cell are engineered to perform a dedicated Boolean function triggered by an appropriate concentration of certain proteins or by different genetic components. These logic circuits work in a manner similar to electronic logic circuits, but they are much more stochastic and hence much harder to characterize. In this article, we introduce an approach to analyze the threshold value and timing of genetic logic circuits. We show how this approach can be used to analyze the timing behavior of single and cascaded genetic logic circuits. We further analyze the timing sensitivity of circuits by varying the degradation rates and concentrations. Our approach can be used not only to characterize the timing behavior but also to analyze the timing constraints of cascaded genetic logic circuits, a capability that we believe will be important for design automation in synthetic biology.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Copenhagen Center for Health Technology
Authors: Baig, H. (Intern), Madsen, J. (Intern)
Number of pages: 11
Pages: 1169-1179
Publication date: 2017
Social Fingerprinting: detection of spambot groups through DNA-inspired behavioral modeling

Spambot detection in online social networks is a long-lasting challenge involving the study and design of detection techniques capable of efficiently identifying ever-evolving spammers. Recently, a new wave of social spambots has emerged, with advanced human-like characteristics that allow them to go undetected even by current state-of-the-art algorithms. In this paper, we show that efficient spambots detection can be achieved via an in-depth analysis of their collective behaviors exploiting the digital DNA technique for modeling the behaviors of social network users. Inspired by its biological counterpart, in the digital DNA representation the behavioral lifetime of a digital account is encoded in a sequence of characters. Then, we define a similarity measure for such digital DNA sequences. We build upon digital DNA and the similarity between groups of users to characterize both genuine accounts and spambots. Leveraging such characterization, we design the Social Fingerprinting technique, which is able to discriminate among spambots and genuine accounts in both a supervised and an unsupervised fashion. We finally evaluate the effectiveness of Social Fingerprinting and we compare it with three state-of-the-art detection algorithms. Among the peculiarities of our approach is the possibility to apply off-the-shelf DNA analysis techniques to study online users behaviors and to efficiently rely on a limited number of lightweight account characteristics.
Microfluidic VLSI (mVLSI) biochips help perform biochemistry at miniaturized scales, thus enabling cost, performance and other benefits. Although biochips are expected to replace biochemical labs, including point-of-care devices, the off-chip pressure actuators and pumps are bulky, thereby limiting them to laboratory environments. To address this issue, researchers have proposed methods to reduce the number of off-chip pressure sources, through integration of on-chip pneumatic control logic circuits fabricated using three-layer monolithic membrane valve technology. Traditionally, mVLSI biochip physical design was performed assuming that all of the control logic is off-chip. However, the problem of mVLSI biochip physical design changes significantly, with introduction of on-chip control, since along with physical synthesis, we also need to (i) perform on/off-chip control partitioning, (ii) on-chip control circuit design and (iii) the integration of on-chip control in the placement and routing design tasks. In this paper we present a design methodology for logic synthesis and physical synthesis of mVLSI biochips that use on-chip control. We show how the proposed methodology can be successfully applied to generate biochip layouts with integrated on-chip pneumatic control.

Synthesis of on-chip control circuits for mVLSI biochips

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Xilinx Asia Pacific, Singapore, spg, Technical University of Denmark
Authors: Potluri, S. (Ekstern), Schneider, A. R. (Intern), Hørslev-Petersen, M. (Ekstern), Pop, P. (Intern), Madsen, J. (Intern)
Pages: 1799-1804
Publication date: 2017

Host publication information
Title of host publication: Proceedings of 20th Design, Automation and Test in Europe
Publisher: IEEE
Article number: 7927284
ISBN (Print): 9783981537093
System-Level Sensitivity Analysis of SiNW-bioFET-Based Biosensing Using Lockin Amplification

Although Silicon Nanowire biological Field-Effect Transistors (SiNW-bioFETs) have steadily demonstrated their ability to detect biological markers at ultra-low concentration, they have not yet translated into routine diagnostics applications. One of the challenges inherent to the technology is that it requires an instrumentation capable of recovering ultra-low signal variations from sensors usually designed and operated in a highly-resistive configuration. Often overlooked, the SiNW-bioFET/ instrument interactions are yet critical factors in determining overall system biodetection performances. Here, we carry out for the first time the system-level sensitivity analysis of a generic SiNW-bioFET model coupled to a custom-design instrument based on the lock-in amplifier. By investigating a large parametric space spanning over both sensor and instrumentation specifications, we demonstrate that systemwide investigations can be instrumental in identifying the design trade-offs that will ensure the lowest Limits-of-Detection. The generic character of our analytical model allows us to elaborate on the most general SiNW-bioFET/instrument interactions and their overall implications on detection performances. Our model can be adapted to better match specific sensor or instrument designs to either ensure that ultra-high sensitivity SiNW-bioFETs are coupled with an appropriately sensitive and noise-rejecting instrumentation, or to best tailor SiNW-bioFET design to the specifications of an existing instrument.

General information
State: Published
Organisations: Department of Management Engineering, Engineering Systems, Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Center for Bachelor of Engineering Studies, Afdelingen for El-teknologi, Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Patou, F. (Intern), Dimaki, M. (Intern), Kjærgaard, C. (Intern), Madsen, J. (Intern), Svendsen, W. E. (Intern)
Pages: 6295-6311
Publication date: 2017
Main Research Area: Technical/natural sciences

Publication information
Journal: IEEE Sensors Journal
Volume: 17
Issue number: 19
ISSN (Print): 1530-437X
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SJR 0.619 SNIP 1.555
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 3.12 SJR 0.654 SNIP 1.683
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.655 SNIP 1.84 CiteScore 2.85
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.775 SNIP 1.894 CiteScore 2.5
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 0.663 SNIP 1.786 CiteScore 2.6
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.663 SNIP 1.616 CiteScore 2.09
ISI indexed (2012): ISI indexed yes
Web of Science (2012): Indexed yes
One of the goals of synthetic biology is to build genetic circuits to control the behavior of a cell for different application domains, such as medical, environmental, and biotech. During the design process of genetic circuits, biologists are often interested in the probability of a system to work under different conditions. Since genetic circuits are noisy and stochastic in nature, the verification process becomes very complicated. The state space of stochastic genetic circuit models is usually too large to be handled by classical model checking techniques. Therefore, the verification of genetic circuit models is usually performed by the statistical approach of model checking. In this work, we present a workflow for checking genetic circuit models using a stochastic model checker (Uppaal) and a stochastic simulator (D-VASim). We demonstrate with experimentations that the proposed workflow is not only sufficient for the model checking of genetic circuits, but can also be used to design the genetic circuits with desired timings.

**General Information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Baig, H. (Intern), Madsen, J. (Intern)
Pages: 503–515
Publication date: 2017

**Host publication information**

Title of host publication: Models, Algorithms, Logics and Tools
Publisher: Springer
ISBN (Print): 9783319631202

Series: Lecture Notes in Computer Science
Volume: 10460
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
Conference: KiMfest, Aalborg, Denmark, 19/08/2017 - 19/08/2017

Electronic versions:

Taming_Living_Logic_using_Formal_Methods_CR.pdf

DOIs:
Test-Driven, Model-Based Systems Engineering.

Hearing systems have evolved over many years from simple mechanical devices (horns) to electronic units consisting of microphones, amplifiers, analog filters, loudspeakers, batteries, etc. Digital signal processors replaced analog filters to provide better performance and new features. Central processors were added to provide many functions for monitoring and controlling other parts of the devices. Hearing systems have thus evolved into complex embedded system. Radio systems were added to allow hearing aids to communicate with accessories, auxiliary equipment, third-party products, etc. Many new features are enabled by such radio communication. Monitoring and controlling hearing aids from remote control devices or smart phones have been incorporated into several products. Direct audio streaming between hearing aids and dedicated streaming devices or smart phones is possible with some products. Also emerging are advanced features that are based on interactions with internet services, clouds, etc. Hearing systems are thus evolving into large and complex smart systems. Designing complex embedded systems or large smart systems are notoriously difficult. Many systems are still developed using document-based methods, where requirements and proposed architecture are described textually with the addition of a few figures and tables. Such documents cannot be subjected to testing, so it is impossible to predict the functionality and performance or even feasibility of the intended systems. Replacing documents with models have several advantages. Models can be simulated and analyzed such that functionality and performance can be predicted before any parts have been built. Potential flaws in the specification can therefore be corrected in early phases, which may reduce development effort and costs. This thesis concerns methods for identifying, selecting and implementing tools for various aspects of model-based systems engineering. A comprehensive method was proposed that include several novel steps such as techniques for analyzing the gap between requirements and tool capabilities. The method was verified with good results in two case studies for selection of a traceability tool (single-tool scenario) and a set of modeling tools (multi-tool scenarios). Models must be subjected to testing to allow engineers to predict functionality and performance of systems. Test-first strategies are known to produce good results in software development. This thesis concerns methods for test-driven modeling of hearing systems. A method is proposed for test-driven modeling of embedded systems of medium complexity. It utilizes formal model checking to guarantee functionality and performance. Test-driven design space exploration is enabled by using statistical model checking to obtain estimates that are verified formally at the final stages of the method. The method was applied with good results to a case study, where two solutions to a design problem were developed and verified. Feasible ranges for critical parameters were identified. Both solution conformed to all requirements. Smart systems are typically too large and complex to be verified by formal model checking, and the research showed that statistical model checking in its current form cannot be used for verifying such systems. A new method is therefore proposed for test-driven modeling of smart systems. The method uses formal verification of basic interactions. Simulations are used for verifying the overall system. To predict performance for scenarios that are too large to be simulated, the method uses mathematical forecasting based on simulating series of smaller scenarios, fitting simulation results to estimator functions, and extrapolating beyond the simulated data set. Mathematical forecasting allowed us to predict the performance of system scenarios that were much too large to be simulated. Such performance estimates may be somewhat imprecise but are nevertheless valuable because they provide answers that cannot be obtained otherwise. The research has thus proposed and verified methods for selecting modeling tools and for test-driven systems modeling for the benefit of GN Hearing and other organizations involved in development of complex embedded systems of large smart systems.
Test-driven modeling and development of cloud-enabled cyber-physical smart systems

Embedded products currently tend to evolve into large and complex smart systems where products are enriched with services through clouds and other web technologies. The complex characteristics of smart systems make it very difficult to guarantee functionality, safety, security and performance. Using test-driven modeling (TDM) is likely to be the best way to design smart systems such that these qualities are ensured. However, the TDM methods that are applied to development of simpler systems do not scale to smart systems because the modeling technologies cannot handle the complexity and size of the systems. In this paper, we present a method for test-driven modeling that scales to very large and complex systems. The method uses a combination of formal verification of basic interactions, simulations of complex scenarios, and mathematical forecasting to predict system behavior and performance. We utilized the method to analyze, design and develop various scenarios for a cloud-enabled medical system. Our approach provides a versatile method that may be adapted and improved for future development of very large and complex smart systems in various domains.
The Internet of Hackable Things

The Internet of Things makes possible to connect each everyday object to the Internet, making computing pervasive like never before. From a security and privacy perspective, this tsunami of connectivity represents a disaster, which makes each object remotely hackable. We claim that, in order to tackle this issue, we need to address a new challenge in security: education.
Timing analysis of rate-constrained traffic in TTEthernet using network calculus

TTEthernet is a deterministic, synchronized and congestion-free network protocol based on the Ethernet standard and compliant with the ARINC 664p7 standard network. It supports safety-critical real-time applications by offering different traffic classes: static time-triggered (TT) traffic, rate-constrained (RC) traffic with bounded end-to-end latencies and best-effort traffic, for which no guarantees are provided. TTEthernet uses three integration policies for sharing the network among the traffic classes: shuffling, preemption and timely block. In this paper, we propose an analysis based on network calculus (NC) to determine the worst-case end-to-end delays of RC traffic in TTEthernet. The main contribution of this paper is capturing the effects of all the integration policies on the latency bounds of RC traffic using NC, and the consideration of relative frame offsets of TT traffic to reduce the pessimism of the RC analysis. The proposed analysis is evaluated on several test cases, including realistic applications (e.g., Orion Crew Exploration Vehicle), and compared to related works.
Timing organization of a real-time multicore processor

Real-time systems need a time-predictable computing platform. Computation, communication, and access to shared resources needs to be time-predictable. We use time division multiplexing to statically schedule all computation and communication resources, such as access to main memory or message passing over a network-on-chip. We use time-driven communication over an asynchronous network-on-chip to enable time division multiplexing even in a globally asynchronous, locally synchronous multicore architecture. Using time division multiplexing at all levels of the architecture yields in a time-predictable multicore processor where we can statically analyze the worst-case execution time of tasks.

Towards industry strength mapping of AUTOSAR automotive functionality on multicore architectures: work in progress

The automotive electronic architectures have moved from federated architectures, where one function is implemented in one ECU (Electronic Control Unit), to distributed architectures, consisting of several multicore ECUs. In addition, multicore ECUs are being adopted because of better performance, cost, size, fault-tolerance and power consumption. Automotive manufacturers use AUTomotive Open System ARchitecture (AUTOSAR) as the standardized software architecture for ECUs. With AUTOSAR, the functionality is modeled as a set of software components composed of subtasks, called runnables. In this paper we propose an approach for the automatic software functionality assignment to multicore distributed architectures, implemented as a software tool. The AUTOMAP, decides: the (i) mapping of software components to multicore ECUs, (ii) the assignment of runnables to the ECU cores, (iii) the clustering of runnables into tasks and (iv) the mapping of tasks to "OS-Applications", such that timing and mapping constraints are satisfied. AUTOMAP has been developed to handle large industrialized use cases, fine-grained realistic mapping and timing constraints, and to produce outputs that support the system engineer in the mapping task. We have successfully evaluated AUTOMAP on several realistic use cases from Volvo Trucks.
Transport or Store? Synthesizing Flow-based Microfluidic Biochips using Distributed Channel Storage

Flow-based microfluidic biochips have attracted much attention in the EDA community due to their miniaturized size and execution efficiency. Previous research, however, still follows the traditional computing model with a dedicated storage unit, which actually becomes a bottleneck of the performance of biochips. In this paper, we propose the first architectural synthesis framework considering distributed storage constructed temporarily from transportation channels to cache fluid samples. Since distributed storage can be accessed more efficiently than a dedicated storage unit and channels can switch between the roles of transportation and storage easily, biochips with this distributed computing architecture can achieve a higher execution efficiency even with fewer resources. Experimental results confirm that the execution efficiency of a bioassay can be improved by up to 28% while the number of valves in the biochip can be reduced effectively.

Volume management for fault-tolerant continuous-flow microfluidics

Recent advancements in microfluidic biochips allow for easier and faster design and fabrication of increasingly complex biochips to replace conventional laboratories. A roadblock in the deployment of biochips however is their low reliability. Physical defects can be introduced during the fabrication process, and may lead to failure of the biochemical application. This can be costly because of the reduced manufacturing yield, the need to redo lengthy experiments, using expensive reagents, and can be safety-critical, e.g., in case of a cancer misdiagnosis. Researchers have started to propose fault models and test techniques for continuous flow biochips. Six typical defects: Block, leak, misalignment, faulty pumps, degradation of valves and dimensional errors have been identified. The resulting faults can be abstracted into blocks and leaks for simplicity. Both fault types can occur in the control-as well as the flow channel, some common causes being environmental particles, imperfections in molds or bubbles in the PDMS gel. While some faults may be detected before the execution of an application by introducing a test run, other faults occur only during runtime as a result of deterioration or...
caused by the applied pressure. If such a fault is detected during runtime, e.g. with a CCD camera, we propose a just in time solution that calculates and assigns fluid volumes to alternate components and routes allowing for the completion of the application despite the occurring fault.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schneider, A. R. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Number of pages: 1
Pages: 102-102
Publication date: 2017

Host publication information
Title of host publication: Proceedings of 2017 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems
Volume: 2017
Publisher: IEEE
ISBN (Print): 9781538603628
Main Research Area: Technical/natural sciences
Conference: 2017 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), Cambridge, United Kingdom, 23/10/2017 - 23/10/2017
Electronic versions:
08244447.pdf
DOIs:
10.1109/DFT.2017.8244447
Source: FindIt
Source-ID: 2395087083
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017

Waste-aware fluid volume assignment for flow-based microfluidic biochips
Microfluidic biochips are replacing the conventional biochemical analysers integrating the necessary functions onchip. We are interested in Flow-Based Microfluidic Biochips (FBMB), where a continuous flow of liquid is manipulated using integrated microvalves. Using microvalves and channels, more complex Fluidic Units (FUs) such as switches, micropumps, mixers and separators can be constructed. When running a biochemical application on a FBMB, fluid volumes are dispensed from input reservoirs and used by the FUs. Given a biochemical application and a biochip, we are interested in determining the fluid volume assignment for each operation of the application, such that the FUs volume requirements are satisfied, while over- and underflow are avoided and the total volume of fluid used is minimized. We propose an algorithm for this fluid assignment problem. Compared to previous work, our method is able to minimize the fluid consumption through optimal fluid assignment and reuse of fluid waste. Due to the algorithm's low complexity, fluid requirements can also be calculated during runtime for error recovery or statically unknown cases.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schneider, A. R. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Pages: 1-6
Publication date: 2017

Host publication information
Title of host publication: 2017 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP)
Publisher: IEEE
ISBN (Print): 9781538629529
Series: 2017 Symposium on Design, Test, Integration and Packaging of Mem/moems (dtip)
Main Research Area: Technical/natural sciences
Conference: 2017 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS, Bordeaux, France, 29/05/2017 - 29/05/2017
Mixers, Biological system modeling, Detectors, Hardware, Microvalves, Fabrication
DOIs:
10.1109/DTIP.2017.7984507
Source: FindIt
Source-ID: 2372483122
Publication: Research - peer-review › Article in proceedings – Annual report year: 2017
A Framework for Dynamically-Loaded Hardware Library (HLL) in FPGA Acceleration

Hardware acceleration is often used to address the need for speed and computing power in embedded systems. FPGAs always represented a good solution for HW acceleration and, recently, new SoC platforms extended the flexibility of the FPGAs by combining on a single chip both high-performance CPUs and FPGA fabric.

The aim of this work is the implementation of hardware accelerators for these new SoCs. The innovative feature of these accelerators is the on-the-fly reconfiguration of the hardware to dynamically adapt the accelerator’s functionalities to the current CPU workload. The realization of the accelerators preliminarily requires also the profiling of both the SW (ARM CPU + NEON Units) and HW (FPGA) performance, an evaluation of the partial reconfiguration times and the development of applicationspecific IP-cores library.

This paper focuses on the profiling aspect of both the SW and HW implementation of the same operations, using arithmetic routines (BLAS) as the reference point for benchmarking, and presents a comparison of the results in terms of speed, power consumption and resources utilization.

A Hardware Framework for on-Chip FPGA Acceleration

In this work, we present a new framework to dynamically load hardware accelerators on reconfigurable platforms (FPGAs). Provided a library of application-specific processors, we load on-the-fly the specific processor in the FPGA, and we transfer the execution from the CPU to the FPGA-based accelerator. Results show that significant speed-up can be obtained by the proposed acceleration framework on system-on-chips where reconfigurable fabric is placed next to the CPUs. The speed-up is due to both the intrinsic acceleration in the application-specific processors, and to the increased parallelism.
A Matter of Words: NLP for Quality Evaluation of Wikipedia Medical Articles

Automatic quality evaluation of Web information is a task with many fields of applications and of great relevance, especially in critical domains, like the medical one. We move from the intuition that the quality of content of medical Web documents is affected by features related with the specific domain. First, the usage of a specific vocabulary (Domain Informativeness); then, the adoption of specific codes (like those used in the infoboxes of Wikipedia articles) and the type of document (e.g., historical and technical ones). In this paper, we propose to leverage specific domain features to improve the results of the evaluation of Wikipedia medical articles, relying on Natural Language Processing (NLP) and dictionaries-based techniques. The results of our experiments confirm that, by considering domain-oriented features, it is possible to improve existing solutions, mainly with those articles that other approaches have less correctly classified.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, IIT-CNR
Authors: Cozza, V. (Ekstern), Petrocchi, M. (Ekstern), Spognardi, A. (Intern)
Number of pages: 9
Pages: 448-456
Publication date: 2016

Host publication information
Title of host publication: Web Engineering: 16th International Conference, ICWE 2016, Lugano, Switzerland, June 6-9, 2016. Proceedings
Volume: 9671
Publisher: Springer
ISBN (Print): 978-3-319-38790-1
ISBN (Electronic): 978-3-319-38791-8

Series: Lecture Notes in Computer Science
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
Conference: The 16th International Conference on Web Engineering (ICWE2016), USI Lugano, Switzerland, 06/06/2016 - 06/06/2016
Information Systems Applications (incl. Internet), Information Storage and Retrieval, Software Engineering, Computer Appl. in Administrative Data Processing, User Interfaces and Human Computer Interaction, Artificial Intelligence (incl. Robotics)
DOIs: 10.1007/978-3-319-38791-8_31
Links: https://arxiv.org/abs/1603.01987
Source: FindIt
Source-ID: 2306622913
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

An Adaptive Middleware for Improved Computational Performance

The performance improvements in computer systems over the past 60 years have been fueled by an exponential increase in energy efficiency. In recent years, the phenomenon known as the end of Dennard’s scaling has slowed energy efficiency improvements — but improving computer energy efficiency is more important now than ever. Traditionally, most improvements in computer energy efficiency have come from improvements in lithography — the ability to produce smaller transistors — and computer architecture - the ability to apply those transistors efficiently. Since the end of scaling, we have seen diminishing returns from developments in lithography and modern computer architectures are so complicated requiring significant programming effort to exploit efficiently — software developers undertaking such a task will need all the help they can get, in order to keep the programming effort down.

In this thesis we champion using software to improve energy efficiency — in particular we develop guidelines for reasoning and evaluating software performance on modern computers, and a middleware that has been designed for modern computers, improving computational performance both in terms of energy and execution time. Our middleware consists of a new power manager, synchronization libraries using hardware transactional memory (for locks, barriers, and task synchronization), and two concurrent map data structures, which can be deployed in computer systems with little to no effort. At a fundamental level, we are improving computational performance by exploiting modern hardware features, such as dynamic voltage-frequency scaling and transactional memory. Adapting software is an iterative process, requiring that we continually revisit it to meet new requirements or realities; a time consuming process which we hope to simplify by analyzing the realities of modern computers, and providing guidelines explaining how to get the most performance out of them.
An Area-Efficient TDM NoC Supporting Reconfiguration for Mode Changes
This paper presents an area-efficient time-division-multiplexing (TDM) network-on-chip (NoC) intended for use in a multicore platform for hard real-time systems. In such a platform, a mode change at the application level requires the tear-down and set-up of some virtual circuits without affecting the virtual circuits that persist across the mode change. Our NoC supports such reconfiguration in a very efficient way, using the same resources that are used for transmission of regular data. We evaluate the presented NoC in terms of worst-case reconfiguration time, hardware cost, and maximum operating frequency. The results show that the hardware cost for an FPGA implementation of our architecture is a factor of 2.2 to 3.9 times smaller than other NoCs with reconfiguration functionalities, and that the worst-case time for a reconfiguration is shorter or comparable to those NoCs.

A Pin-Count Reduction Algorithm for Flow-Based Microfluidic Biochips
Microfluidic biochips are replacing the conventional biochemical analyzers integrating the necessary functions on-chip. We are interested in flow-based biochips, where a continuous flow of liquid is manipulated using integrated microvalves, controlled from external pressure sources via off-chip control pins. Recent research has addressed the physical design of such biochips. However, such research has so far ignored the pin-count, which rises with the increase in the number of microvalves. Given a biochip architecture and a biochemical application, we propose an algorithm for reducing the number of control pins required to run the application. The proposed algorithm has been evaluated using several benchmarks.
Architecture Synthesis for Cost-Constrained Fault-Tolerant Flow-based Biochips

In this paper, we are interested in the synthesis of fault-tolerant architectures for flow-based microfluidic biochips, which use microvalves and channels to run biochemical applications. The growth rate of device integration in flow-based microfluidic biochips is scaling faster than Moore's law. This increase in fabrication complexity has led to an increase in defect rates during the manufacturing, thereby motivating the need to improve the yield, by designing these biochips such that they are fault tolerant. We propose an approach based on a Greedy Randomized Adaptive Search Procedure (GRASP) for the synthesis of fault-tolerant biochip architectures. Our approach optimizes the introduction of redundancy within a given unit cost budget, such that, the biochemical application can successfully complete its execution within its deadline, even in the presence of faults, and the yield is maximized. The proposed algorithm has been evaluated using several benchmarks and compared to the results of a Simulated Annealing metaheuristic.

Argo: A Real-Time Network-on-Chip Architecture With an Efficient GALS Implementation

In this paper, we present an area-efficient, globally asynchronous, locally synchronous network-on-chip (NoC) architecture for a hard real-time multiprocessor platform. The NoC implements message-passing communication between processor cores. It uses statically scheduled time-division multiplexing (TDM) to control the communication over a structure of routers, links, and network interfaces (NIs) to offer real-time guarantees. The area-efficient design is a result of two contributions: 1) asynchronous routers combined with TDM scheduling and 2) a novel NI microarchitecture. Together they result in a design in which data are transferred in a pipelined fashion, from the local memory of the sending core to the local memory of the receiving core, without any dynamic arbitration, buffering, and clock synchronization. The routers use two-phase bundled-data handshake latches based on the Mousetrap latch controller and are extended with a clock gating mechanism to reduce the energy consumption. The NIs integrate the direct memory access functionality and the TDM schedule, and use dual-ported local memories to avoid buffering, flow-control, and synchronization. To verify the design,
we have implemented a 4 x 4 bitorus NoC in 65-nm CMOS technology and we present results on area, speed, and energy consumption for the router, NI, NoC, and postlayout.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Eindhoven University of Technology
Authors: Kasapaki, E. (Intern), Schoeberl, M. (Intern), Sørensen, R. B. (Intern), Müller, C. (Intern), Goossens, K. (Ekstern), Sparso, J. (Intern)
Pages: 479-492
Publication date: 2016
Main Research Area: Technical/natural sciences

**Publication information**

Journal: IEEE Transactions on Very Large Scale Integration (VLSI) Systems
Volume: 24
Issue number: 2
ISSN (Print): 1063-8210
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 1.56 SJR 0.447
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): SJR 0.411 SNIP 1.829 CiteScore 2.25
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.592 SNIP 2.289 CiteScore 2.47
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.552 SNIP 1.887 CiteScore 2.17
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 0.528 SNIP 1.833 CiteScore 2.13
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.534 SNIP 1.747 CiteScore 2.07
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.557 SNIP 1.575 CiteScore 2.14
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.474 SNIP 1.36
BFI (2009): BFI-level 2
Scopus rating (2009): SJR 0.586 SNIP 1.547
Web of Science (2009): Indexed yes
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.636 SNIP 1.485
Scopus rating (2007): SJR 0.729 SNIP 1.792
Scopus rating (2006): SJR 0.722 SNIP 1.867
Scopus rating (2005): SJR 0.687 SNIP 2.026
Scopus rating (2004): SJR 0.655 SNIP 1.939
Web of Science (2004): Indexed yes
Scopus rating (2003): SJR 0.97 SNIP 1.843
Scopus rating (2002): SJR 1.28 SNIP 2.358
Scopus rating (2001): SJR 0.968 SNIP 1.868
Scopus rating (2000): SJR 0.362 SNIP 1.865
Web of Science (2000): Indexed yes
A scalable lock-free hash table with open addressing
Concurrent data structures synchronized with locks do not scale well with the number of threads. As more scalable alternatives, concurrent data structures and algorithms based on widely available, however advanced, atomic operations have been proposed. These data structures allow for correct and concurrent operations without any locks. In this paper, we present a new fully lock-free open addressed hash table with a simpler design than prior published work. We split hash table insertions into two atomic phases: first inserting a value ignoring other concurrent operations, then in the second phase resolve any duplicate or conflicting values.

Our hash table has a constant and low memory usage that is less than existing lock-free hash tables at a fill level of 33% and above. The hash table exhibits good cache locality. Compared to prior art, our hash table results in 16% and 15% fewer L1 and L2 cache misses respectively, leading to 21% fewer memory stall cycles. Our experiments show that our hash table scales close to linearly with the number of threads and outperforms, in throughput, other lock-free hash tables by 19%.

A Software Managed Stack Cache for Real-Time Systems
In a real-time system, the use of a scratchpad memory can mitigate the difficulties related to analyzing data caches, whose behavior is inherently hard to predict. We propose to use a scratchpad memory for stack allocated data. While statically allocating stack frames for individual functions to scratchpad memory regions aids predictability, it is limited to non-recursive programs and static allocation has to take different calling contexts into account. Using a stack cache that dynamically spills data to and fills data from external memory avoids these problems, while its simple design allows for efficiently deriving worst-case bounds through static analysis.

In this paper we present the design and implementation of software managed caching of stack allocated data in a scratchpad memory. We demonstrate a compiler-aided implementation of a stack cache using the LLVM compiler framework and report on its efficiency. Our evaluation encompasses stack management overhead and impact on worst-case execution time analysis. The state-of-the-art worst-case execution time analysis tool aiT is able to correctly classify all stack cache accesses as accesses to the scratchpad memory.
A Stack Cache for Real-Time Systems

Real-time systems need time-predictable computing platforms to allow for static analysis of the worst-case execution time. Caches are important for good performance, but data caches are hard to analyze for the worst-case execution time. Stack allocated data has different properties related to locality, lifetime, and static analyzability of access addresses compared to static or heap allocated data. Therefore, caching of stack allocated data benefits from having its own cache.

In this paper, we present a cache architecture optimized for stack allocated data. This cache is additional to the normal data cache. As stack allocated data has a high locality, even a small stack cache gives a high hit rate. A stack cache added to a write-through data cache considerably improves the performance, while a stack cache compared to the harder to analyze write-back cache has about the same average case performance.

A Survey of Man in the Middle Attacks

The Man-In-The-Middle (MITM) attack is one of the most well-known attacks in computer security, representing one of the biggest concerns for security professionals. MITM targets the actual data that flows between endpoints, and the confidentiality and integrity of the data itself. In this paper, we extensively review the literature on MITM to analyze and categorize the scope of MITM attacks, considering both a reference model, such as the open systems interconnection (OSI) model, as well as two specific widely used network technologies, i.e., GSM and UMTS. In particular, we classify MITM attacks based on several parameters, like location of an attacker in the network, nature of a communication channel, and impersonation techniques. Based on an impersonation techniques classification, we then provide execution steps for each MITM class. We survey existing countermeasures and discuss the comparison among them. Finally, based on our analysis, we propose a categorization of MITM prevention mechanisms, and we identify some possible directions for future research.
Automatic Functionality Assignment to AUTOSAR Multicore Distributed Architectures

The automotive electronic architectures have moved from federated architectures, where one function is implemented in one ECU (Electronic Control Unit), to distributed architectures, where several functions may share resources on an ECU. In addition, multicore ECUs are being adopted because of better performance, cost, size, fault-tolerance and power consumption. In this paper we present an approach for the automatic software functionality assignment to multicore distributed architectures. We consider that the systems use the AUTomotive Open System ARchitecture (AUTOSAR). The
functionality is modeled as a set of software components composed of subtasks, called runnables, in AUTOSAR terminology. We have proposed a Simulated Annealing metaheuristic optimization that decides: (i) the mapping of software components to multicore ECUs, (ii) the assignment of runnables to the ECU cores, (iii) the clustering of runnables into tasks and (iv) the mapping of tasks to “OS-Applications” (used to isolate mixed safety-criticality functions). We are interested to determine an implementation such that (1) the mapping constraints are satisfied, (2) the runnables are schedulable and (3) they are spatially and temporally isolated if they have different safety-criticality levels, (4) the overall communication bandwidth is minimized and (5) the utilization of the cores and ECUs is balanced. The proposed approach was evaluated on three realistic case studies.

General information
State: Published
Organisations: Department of Chemical and Biochemical Engineering, Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Volvo Group Trucks Technology
Authors: Maticu, F. (Intern), Pop, P. (Intern), Axbrink, C. (Ekstern), Islam, M. (Ekstern)
Number of pages: 11
Publication date: 2016

Avionics Applications on a Time-Predictable Chip-Multiprocessor
Avionics applications need to be certified for the highest criticality standard. This certification includes schedulability analysis and worst-case execution time (WCET) analysis. WCET analysis is only possible when the software is written to be WCET analyzable and when the platform is time-predictable. In this paper we present prototype avionics applications that have been ported to the time-predictable T-CREST platform. The applications are WCET analyzable, and T-CREST is supported by the aiT WCET analyzer. This combination allows us to provide WCET bounds of avionic tasks, even when executing on a multicore processor.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, GMV
Authors: Rocha, A. (Ekstern), Silva, C. (Ekstern), Sørensen, R. B. (Intern), Sparsø, J. (Intern), Schoeberl, M. (Intern)
Pages: 777-785
Publication date: 2016

Behavioral activities collected through smartphones and the association with illness activity in bipolar disorder
Smartphones are useful in symptom-monitoring in bipolar disorder (BD). Objective smartphone data reflecting illness activity could facilitate early treatment and act as outcome in efficacy trials. A total of 29 patients with BD presenting with moderate to severe levels of depressive and manic symptoms used a smartphone-based self-monitoring system during 12
weeks. Objective smartphone data on behavioral activities were collected. Symptoms were clinically assessed every
second week using the Hamilton Depression Rating Scale and the Young Mania Rating Scale. Objective smartphone data
were symptom severity. The more severe the depressive symptoms (1) the longer the smartphone’s screen was
“on”/day, (2) more received incoming calls/day, (3) fewer outgoing calls/day were made, (4) less answered incoming
calls/day, (5) the patients moved less between cell towers IDs/day. Conversely, the more severe the manic symptoms (1)
more outgoing text messages/day sent, (2) the phone calls/day were longer, (3) the fewer number of characters in
incoming text messages/day, (4) the lower duration of outgoing calls/day, (5) the patients moved more between cell towers
IDs/day. Further, objective smartphone data were able to discriminate between affective states. Objective smartphone
data reflect illness severity, discriminates between affective states in BD and may facilitate the cooperation between
patient and clinician.

General information
State: Published
Organisations: Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science ,
Embedded Systems Engineering, Psychiatric Center Copenhagen, Rigshospitalet, IT University of Copenhagen
Authors: Faurholt-Jepsen, M. (Ekstern), Vinberg, M. (Ekstern), Frost, M. (Ekstern), Debel, S. (Ekstern), Christensen, E. M. (Ekstern),
Bardram, J. E. (Intern), Kessing, L. V. (Ekstern)
Number of pages: 15
Pages: 309–323
Publication date: 2016
Main Research Area: Technical/natural sciences

Publication Information
Volume: 25
Issue number: 4
ISSN (Print): 1557-0657
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 1.53 SJR 1.297
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 3 SJR 1.645 SNIP 1.669
Scopus rating (2015): SJR 2.373 SNIP 1.774 CiteScore 4.09
Scopus rating (2014): SJR 2.448 SNIP 1.859 CiteScore 3.91
Scopus rating (2013): SJR 1.374 SNIP 1.663 CiteScore 3.34
Scopus rating (2012): SJR 1.673 SNIP 1.231 CiteScore 2.52
Scopus rating (2011): SJR 1.638 SNIP 1.406 CiteScore 2.95
Scopus rating (2010): SJR 1.713 SNIP 1.411
Scopus rating (2009): SJR 1.567 SNIP 1.174
Scopus rating (2008): SJR 0.823 SNIP 0.646
Scopus rating (2007): SJR 3.688 SNIP 2.294
Scopus rating (2006): SJR 2.924 SNIP 2.076
Scopus rating (2005): SJR 2.404 SNIP 1.845
Scopus rating (2004): SJR 1.126 SNIP 0.962
Scopus rating (2003): SJR 0.682 SNIP 0.551
Scopus rating (2002): SJR 0.734 SNIP 0.573
Scopus rating (2001): SJR 0.402 SNIP 0.392
Scopus rating (2000): SJR 0.94 SNIP 0.668
Scopus rating (1999): SJR 0.761 SNIP 0.872
Original language: English
Bipolar disorder, Smartphone, Illness activity, Automatically generated objective data, Objective outcome measure
DOIs:
10.1002/mpr.1502
Source: PublicationPreSubmission
Source-ID: 123340419
Publication: Research - peer-review › Journal article – Annual report year: 2016

Bioinspired Security Analysis of Wireless Protocols
Fraglets represent an execution model for communication protocols that resembles the chemical reactions in living
organisms. The strong connection between their way of transforming and reacting and formal rewriting systems makes a
fraglet program amenable to automatic verification. Grounded on past work, this paper investigates feasibility of adopting fraglets as model for specifying security protocols and analysing their properties. In particular, we give concrete sample analyses over a secure RFID protocol, showing evolution of the protocol run as chemical dynamics and simulating an adversary trying to circumvent the intended steps. The results of our analysis confirm the effectiveness of the cryptofraglets framework for the model and analysis of security properties and eventually show its potential to identify and uncover protocol flaws.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, CNR Institute of Informatics and Telematics, Massachusetts Institute of Technology
Authors: Petrocchi, M. (Ekstern), Spognardi, A. (Intern), Santi, P. (Ekstern)
Pages: 139-148
Publication date: 2016
Main Research Area: Technical/natural sciences

Publication information
Journal: Mobile Networks and Applications
Volume: 21
Issue number: 1
ISSN (Print): 1383-469X
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 2.015 SJR 0.634
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): SJR 0.613 SNIP 1.794 CiteScore 3.48
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.551 SNIP 1.658 CiteScore 2.29
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.528 SNIP 1.836 CiteScore 2.09
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.555 SNIP 1.677 CiteScore 2.18
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.593 SNIP 1.937 CiteScore 2.06
BFI (2011): BFI-level 1
Scopus rating (2011): SJR 0.478 SNIP 1.382 CiteScore 1.69
BFI (2010): BFI-level 1
Scopus rating (2010): SJR 0.463 SNIP 1.462
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.865 SNIP 2.179
BFI (2008): BFI-level 1
Scopus rating (2008): SJR 0.96 SNIP 2.373
Scopus rating (2007): SJR 0.75 SNIP 2.075
Scopus rating (2006): SJR 0.781 SNIP 2.194
Scopus rating (2005): SJR 0.916 SNIP 2.207
Scopus rating (2004): SJR 1.055 SNIP 2.242
Scopus rating (2003): SJR 0.83 SNIP 1.787
Scopus rating (2002): SJR 1.099 SNIP 1.713
Scopus rating (2001): SJR 1.095 SNIP 1.943
Scopus rating (2000): SJR 1.063 SNIP 1.132
Scopus rating (1999): SJR 0.939 SNIP 1.056
Original language: English
Fraglets, Secure RFID protocols, Maude
DOIs:
Clock domain crossing modules for OCP-style read/write interfaces
The open core protocol (OCP) is an openly licensed, configurable, and scalable interface protocol for on-chip subsystem communications. The protocol defines read and write transactions from a master towards a slave across a point-to-point connection and the protocol assumes a single common clock.

This paper presents the design of two OCP clock domain crossing interface modules, that can be used to construct systems with multiple clock domains. One module (called OCPio) supports a single word read-write interface and the other module (called OCPburst) supports a four word burst read-write interface.

The modules has been developed for the T-CREST multi-core platform [8, 9, 13] but they can easily be adopted and used in other designs implementing variants of the OCP interface standard. The OCPio module is used to connect a Patmos processor to a message passing network-on-chip and the OCPburst is used to connect the Processor and its cache controllers to a shared o_-chip memory.

While the problem of synchronizing a simple streaming interface is well described in the literature and often solved using bi-synchronous FIFOs we found surprisingly little published material addressing synchronization of bus-style read-write transaction interfaces. An OCP interface typically has control signals related to both the master issuing a read or write request and the slave producing a response. If all these control signals are passed across the clock domain boundary and synchronized it may add significant latency to the duration of a transaction. Our interface designs avoid this and synchronize only a single signal transition in each direction during a read or a write transaction. The designs are available as open source, and the modules have been tested in a complete multi-core platform implemented on an FPGA board.
Memristors were theorized more than fifty years ago, but only recently physical devices with memristor's behavior have been fabricated and shipped. In this work, we experiment on one of these physical memristors by designing a memristor-based memory cell, implementing the cell, and testing it. Our experiments demonstrate that the memristor technology is not yet mature for practical applications, but, nevertheless, when production will provide reliable and dependable devices, memristor-based memory systems may replace CMOS memories with some advantages.
Designing Context-Aware Cognitive Behavioral Therapy for Unipolar and Bipolar Disorders
This position paper presents our preliminary design of context-aware cognitive behavioral therapy for unipolar and bipolar disorders. We report on the background for this study and the methods applied in the ongoing design process. The paper ends by presenting and discussing different design options. We hope this will be useful input for further discussion at the workshop.

Design optimization for security-and safety-critical distributed real-time applications
In this paper, we are interested in the design of real-time applications with security, safety, timing, and energy requirements. The applications are scheduled with cyclic scheduling, and are mapped on distributed heterogeneous architectures. Cryptographic services are deployed to satisfy security requirements on confidentiality of messages, task replication is used to enhance system reliability, and dynamic voltage and frequency scaling is used for energy efficiency of tasks. It is challenging to address these factors simultaneously, e.g., better security protections need more computing resources and consume more energy, while lower voltages and frequencies may impair schedulability and security, and also lead to reliability degradation. We introduce a vulnerability based method to quantify the security performance of communications on distributed systems. We then focus on determining the appropriate security measures for messages, the voltage and frequency levels for tasks, and the schedule tables such that the security and reliability requirements are satisfied, the application is schedulable, and the energy consumption is minimized. We propose a Tabu Search based metaheuristic to solve this problem. Extensive experiments and a real-life application are conducted to evaluate the proposed techniques.
**Design Optimization of Cyber-Physical Distributed Systems using IEEE Time-sensitive Networks (TSN)**

In this paper we are interested in safety-critical real-time applications implemented on distributed architectures supporting the Time-Sensitive Networking (TSN) standard. The ongoing standardization of TSN is an IEEE effort to bring deterministic real-time capabilities into the IEEE 802.1 Ethernet standard supporting safety-critical systems and guaranteed Quality-of-Service. TSN will support Time-Triggered (TT) communication based on schedule tables, Audio-Video-Bridging (AVB) flows with bounded end-to-end latency as well as Best-Effort messages. We first present a survey of research related to the optimization of distributed cyber-physical systems using real-time Ethernet for communication. Then, we formulate two novel optimization problems related to the scheduling and routing of TT and AVB traffic in TSN. Thus, we consider that we know the topology of the network as well as the set of TT and AVB flows. We are interested to determine the routing of both TT and AVB flows as well as the scheduling of the TT flows such that all frames are schedulable and the AVB worst-case end-to-end delay is minimized. We have proposed an Integer Linear Programming (ILP) formulation for the scheduling problem and a Greedy Randomized Adaptive Search Procedure (GRASP)-based heuristic for the routing problem. The proposed approaches have been evaluated using several test cases.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, TTTech Computertechnik AG, Technical University of Denmark
Authors: Pop, P. (Intern), Lander Raagaard, M. (Ekstern), Craciunas, S. S. (Ekstern), Steiner, W. (Ekstern)
Number of pages: 21
Pages: 86-94
Publication date: 2016
Main Research Area: Technical/natural sciences

**Publication information**

Journal: IET Cyber-Physical Systems: Theory and Applications
Volume: 1
Issue number: 1
ISSN (Print): 2398-3396
Original language: English
Electronic versions:
paupo_ietcps16_v3_1.pdf
DOIs:
10.1049/iet-cps.2016.0021

**Bibliographical note**

This is an open access article published by the IET under the Creative Commons Attribution-NonCommercial-NoDerivs License (http://creativecommons.org/licenses/by-nc-nd/3.0/)

Source: PublicationPreSubmission
Source-ID: 127146953
Publication: Research - peer-review › Journal article – Annual report year: 2016

**Discounted Duration Calculus**

To formally reason about the temporal quality of systems discounting was introduced to CTL and LTL. However, these logic are discrete and they cannot express duration properties. In this work we introduce discounting for a variant of Duration Calculus. We prove decidability of model checking for a useful fragment of discounted Duration Calculus formulas on timed automata under mild assumptions. Further, we provide an extensive example to show the usefulness of the fragment.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Oldenburg
Authors: Ody, H. (Ekstern), Fränzle, M. (Ekstern), Hansen, M. R. (Intern)
Pages: 577-592
Publication date: 2016

**Host publication information**

Title of host publication: Proceedings of the 21st International Symposium on Formal Methods (FM 2016)
DNA-Inspired Online Behavioral Modeling and Its Application to Spambot Detection

A novel, simple, and effective approach to modeling online user behavior extracts and analyzes digital DNA sequences from user online actions and uses Twitter as a benchmark to test the proposal. Specifically, the model obtains an incisive and compact DNA-inspired characterization of user actions. Then, standard DNA analysis techniques discriminate between genuine and spambot accounts on Twitter. An experimental campaign supports the proposal, showing its effectiveness and viability. Although Twitter spambot detection is a specific use case on a specific social media platform, the proposed methodology is platform and technology agnostic, paving the way for diverse behavioral characterization tasks.
D-VASim: An Interactive Virtual Laboratory Environment for the Simulation and Analysis of Genetic Circuits

Simulation and behavioral analysis of genetic circuits is a standard approach of functional verification prior to their physical implementation. Many software tools have been developed to perform in silico analysis for this purpose, but none of them allow users to interact with the model during runtime. The runtime interaction gives the user a feeling of being in the lab performing a real world experiment. In this work, we present a user-friendly software tool named D-VASim (Dynamic Virtual Analyzer and Simulator), which provides a virtual laboratory environment to simulate and analyze the behavior of genetic logic circuit models represented in an SBML (Systems Biology Markup Language). Hence, SBML models developed in other software environments can be analyzed and simulated in D-VASim. D-VASim offers deterministic as well as stochastic simulation; and differs from other software tools by being able to extract and validate the Boolean logic from the SBML model. D-VASim is also capable of analyzing the threshold value and propagation delay of a genetic circuit model.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Baig, H. (Intern), Madsen, J. (Intern)
Number of pages: 3
Pages: 297-299
Publication date: 2016
Main Research Area: Technical/natural sciences

Publication information
Journal: Bioinformatics
Volume: 33
Issue number: 2
ISSN (Print): 1367-4803
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 2
D-VASim: A Software Tool to Simulate and Analyze Genetic Logic Circuits

The Challenge:
Creating a software tool for the simulation and analysis of genetic logic circuits to help researchers performing wet lab experiments virtually, because the manual process of wet lab experimentation of genetic logic circuits is time consuming and a challenging task for early-stage researchers with limited experience in the field of biology.

The Solution:
Using LabVIEW to develop a user-friendly simulation tool named Dynamic Virtual Analyzer and Simulator (D-VASim), which is the first software tool in the domain of synthetic biology that provides a virtual laboratory environment to perform run-time interactive simulation and analysis of genetic logic circuits.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Baig, H. (Intern), Madsen, J. (Intern)
Publication date: 2016
Dynamically-Loaded Hardware Libraries (HLL) Technology for Audio Applications

In this work, we apply hardware acceleration to embedded systems running audio applications. We present a new framework, Dynamically-Loaded Hardware Libraries or HLL, to dynamically load hardware libraries on reconfigurable platforms (FPGAs). Provided a library of application-specific processors, we load on-the-fly the specific processor in the FPGA, and we transfer the execution from the CPU to the FPGA-based accelerator. The proposed architecture provides excellent flexibility with respect to the different audio applications implemented, high quality audio, and an energy efficient solution.

Efficient Worst-Case Execution Time Analysis of Dynamic Branch Prediction

Dynamic branch prediction is commonly found in modern processors, but notoriously difficult to model for worst-case execution time analysis. This is particularly true for global dynamic branch predictors, where predictions are influenced by the global branch history. Prior research in this area has concluded that modeling of global branch prediction is too costly for practical use. This paper presents an approach to model global branch prediction while keeping the analysis effort reasonably low. The approach separates the branch history analysis from the integer linear programming formulation of the worst-case execution time problem. Consequently, the proposed approach scales to longer branch history lengths than previous approaches.
Electronic self-monitoring of mood using IT platforms in adult patients with bipolar disorder: A systematic review of the validity and evidence

Background: Various paper-based mood charting instruments are used in the monitoring of symptoms in bipolar disorder. During recent years an increasing number of electronic self-monitoring tools have been developed. The objectives of this systematic review were 1) to evaluate the validity of electronic self-monitoring tools as a method of evaluating mood compared to clinical rating scales for depression and mania and 2) to investigate the effect of electronic self-monitoring tools on clinically relevant outcomes in bipolar disorder.

Methods: A systematic review of the scientific literature, reported according to the Preferred Reporting items for Systematic Reviews and Meta-Analysis (PRISMA) guidelines was conducted. MEDLINE, Embase, PsycINFO and The Cochrane Library were searched and supplemented by hand search of reference lists. Databases were searched for 1) studies on electronic self-monitoring tools in patients with bipolar disorder reporting on validity of electronically self-reported mood ratings compared to clinical rating scales for depression and mania and 2) randomized controlled trials (RCT) evaluating electronic mood self-monitoring tools in patients with bipolar disorder.

Results: A total of 13 published articles were included. Seven articles were RCTs and six were longitudinal studies. Electronic self-monitoring of mood was considered valid compared to clinical rating scales for depression in six out of six studies, and in two out of seven studies compared to clinical rating scales for mania. The included RCTs primarily investigated the effect of heterogeneous electronically delivered interventions; none of the RCTs investigated the sole effect of electronic mood self-monitoring tools. Methodological issues with risk of bias at different levels limited the evidence in the majority of studies.

Conclusions: Electronic self-monitoring of mood in depression appears to be a valid measure of mood in contrast to self-monitoring of mood in mania. There are yet few studies on the effect of electronic self-monitoring of mood in bipolar disorder. The evidence of electronic self-monitoring is limited by methodological issues and by a lack of RCTs. Although the idea of electronic self-monitoring of mood seems appealing, studies using rigorous methodology investigating the beneficial as well as possible harmful effects of electronic self-monitoring are needed.
Strong passwords have been preached since decades. However, a lot of the regular users of IT systems resort to simple and repetitive passwords, especially nowadays in the "service era". To help alleviate this problem, a new class of software grew popular: password managers. Since their introduction, password managers have slowly been migrating into the cloud. In this paper we review and analyze current professional password managers in the cloud. We discuss several functional and nonfunctional requirements to evaluate existing solutions and we sum up their strengths and weaknesses. The main conclusion is that a silver bullet solution is not available yet and that this type of tools still deserve a significant research effort from the privacy and security community.
Evolvable Smartphone-Based Platforms for Point-Of-Care In-Vitro Diagnostics Applications

The association of smart mobile devices and lab-on-chip technologies offers unprecedented opportunities for the emergence of direct-to-consumer in vitro medical diagnostics applications. Despite their clear transformative potential, obstacles remain to the large-scale disruption and long-lasting success of these systems in the consumer market. For instance, the increasing level of complexity of instrumented lab-on-chip devices, coupled to the sporadic nature of point-of-care testing, threatens the viability of a business model mainly relying on disposable/consumable lab-on-chips. We argued recently that system evolvability, defined as the design characteristic that facilitates more manageable transitions between system generations via the modification of an inherited design, can help remedy these limitations. In this paper, we discuss how platform-based design can constitute a formal entry point to the design and implementation of evolvable smart device/lab-on-chip systems. We present both a hardware/software design framework and the implementation details of a platform prototype enabling at this stage the interfacing of several lab-on-chip variants relying on current- or impedance-based biosensors. Our findings suggest that several change-enabling mechanisms implemented in the higher abstraction software layers of the system can promote evolvability, together with the design of change-absorbing hardware/software interfaces. Our platform architecture is based on a mobile software application programming interface coupled to a modular hardware accessory. It allows the specification of lab-on-chip operation and post-analytic functions at the mobile software layer. We demonstrate its potential by operating a simple lab-on-chip to carry out the detection of dopamine using various electroanalytical methods.
Experimental Measures of News Personalization in Google News
Search engines and social media keep trace of profile- and behavioral-based distinct signals of their users, to provide
them personalized and recommended content. Here, we focus on the level of web search personalization, to estimate the
risk of trapping the user into so called Filter Bubbles. Our experimentation has been carried out on news, specifically
investigating the Google News platform. Our results are in line with existing literature and call for further analyses on which
kind of users are the target of specific recommendations by Google.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, IMT School
for Advanced Studies Lucca, IIT-CNR
Authors: Cozza, V. (Ekstern), Hoang, V. T. (Ekstern), Petrocchi, M. (Ekstern), Spognardi, A. (Intern)
Pages: 93-104
Publication date: 2016

Host publication information
Title of host publication: Current Trends in Web Engineering: Revised Selected Papers from the ICWE 2016 International
Workshops DUI, TELERISE, SoWeMine, and Liquid Web
Publisher: Springer
ISBN (Print): 978-3-319-46962-1
ISBN (Electronic): 978-3-319-46963-8
Series: Lecture Notes in Computer Science
Volume: 9881
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
Conference: 2nd International Workshop on TEchnical and LEGal aspects of data pRivacy and SEcurity (TELERISE 2016), USI Lugano, Switzerland, 09/06/2016 - 09/06/2016
Filter bubbles, Web search results, News publishers
DOIs:
10.1007/978-3-319-46963-8_8
Source: FindIt
Source-ID: 2348930985
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

FMI for Co-Simulation of Embedded Control Software
Increased complexity of cyber-physical systems within the maritime industry demands closer cooperation be-tween
engineering disciplines. The functional mockup interface (FMI) is an initiative aiding cross-discipline in-teraction by
providing, a widely accepted, standard for model exchange and co-simulation. The standard is sup-ported by a number of
modelling tools. However, to im-plement it on an existing platform requires adaptation. This paper investigates how to
adapt the software of an embedded control system to comply with the FMI for co-simulation standard. In particular, we
suggest a way of advancing the clock of a real time operating system (RTOS), by overwriting the idle thread and waiting
for a signal to start execution until return to idle. This ap-proach ensures a deterministic and temporal execution of the
simulation across multiple nodes. As proof of concept, a co-simulation is conducted, showing that the control system of an
SCR (selective catalyst reduction) emission reduction system can be packed in a functional mockup unit (FMU) and co-
simulated with a physical model, built in Ptolemy II. Results show that FMI can be used for co-simulation of an embedded
SCR control soft-ware and for control software development.

General information
FPGA Acceleration by Dynamically-Loaded Hardware Libraries

Hardware acceleration is a viable solution to obtain energy efficiency in data intensive computation.

In this work, we present a hardware framework to dynamically load hardware libraries, HLL, on reconfigurable platforms (FPGAs). Provided a library of application-specific processors, we load on-the-fly the specific processor in the FPGA, and we transfer the execution from the CPU to the FPGA-based accelerator.

Results show that significant speed-up and energy efficiency can be obtained by HLL acceleration on system-on-chips where reconfigurable fabric is placed next to the CPUs.

Game-based verification and synthesis

Infinite-duration games provide a convenient way to model distributed, reactive and open systems in which several entities and an uncontrollable environment interact. Here, each entity as well as the uncontrollable environment are modelled as players.

A strategy for an entity player in the model corresponds directly to a program for the corresponding entity of the system. A
strategy for a player which ensures that the player wins no matter how the other players behave then corresponds to a program ensuring that the specification of the entity is satisfied no matter how the other entities and the environment behaves. Synthesis of strategies in games can thus be used for automatic generation of correct-by-construction programs from specifications.

We consider verification and synthesis problems for several well-known game-based models. This includes both model-checking problems and satisfiability problems for logics capable of expressing strategic abilities of players in games with both qualitative and quantitative objectives.

A number of computational complexity results for model-checking and satisfiability problems in this domain are obtained. We also show how the technique of symmetry reduction can be extended to solve finitely-branching turn-based games more efficiently. Further, the novel concept of winning cores in parity games is introduced. We use this to develop a new polynomial-time under-approximation algorithm for solving parity games. Experimental results show that this algorithm performs better than the state-of-the-art algorithms in most benchmark games.

Two new game-based modelling formalisms for distributed systems are presented. The first makes it possible to reason about systems where several identical entities interact. The second provides a game-based modelling formalism for distributed systems with continuous time and probability distributions over the duration of delays. For these new models we provide decidability and undecidability results for problems concerning computation of symmetric Nash equilibria and for deciding existence of strategies that ensure reaching a target with a high probability.
Implementation of Hardware Accelerators on Zynq

In the recent years it has become obvious that the performance of general purpose processors are having trouble meeting the requirements of high performance computing applications of today. This is partly due to the relatively high power consumption, compared to the performance, of general purpose processors, which has made hardware accelerators an essential part of several datacentres and the worlds fastest super-computers.

In this work, two different hardware accelerators were implemented on a Xilinx Zynq SoC platform mounted on the ZedBoard platform. The two accelerators are based on two different benchmarks, a Monte Carlo simulation of European stock options and a Telco telephone billing application. Each of the accelerators test different aspects of the Zynq platform in terms of floating-point and binary coded decimal processing speed. The two accelerators are compared with the performance of the ARM Cortex-9 processor featured on the Zynq SoC, with regard to execution time, power dissipation and energy consumption.

The implementation of the hardware accelerators were successful. Use of the Monte Carlo processor resulted in a significant increase in performance. The Telco hardware accelerator showed a very high increase in performance over the ARM-processor.

Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction

In this paper, we describe an optimization for binary radix-16 (modified) Booth recoded multipliers to reduce the maximum height of the partial product columns to \(\left\lceil \frac{n}{4} \right\rceil\) for unsigned operands. This is in contrast to the conventional maximum height of \(\left\lceil \frac{n+1}{4} \right\rceil\). Therefore, a reduction of one unit in the maximum height is achieved. This reduction may add flexibility during the design of the pipelined multiplier to meet the design goals, it may allow further optimizations of the partial product array reduction stage in terms of area/delay/power and/or may allow additional addends to be included in the partial product array without increasing the delay. The method can be extended to Booth recoded radix-8 multipliers, signed multipliers, combined signed/unsigned multipliers, and other values of n.

Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction

In this paper, we describe an optimization for binary radix-16 (modified) Booth recoded multipliers to reduce the maximum height of the partial product columns to \(\left\lceil \frac{n}{4} \right\rceil\) for unsigned operands. This is in contrast to the conventional maximum height of \(\left\lceil \frac{n+1}{4} \right\rceil\). Therefore, a reduction of one unit in the maximum height is achieved. This reduction may add flexibility during the design of the pipelined multiplier to meet the design goals, it may allow further optimizations of the partial product array reduction stage in terms of area/delay/power and/or may allow additional addends to be included in the partial product array without increasing the delay. The method can be extended to Booth recoded radix-8 multipliers, signed multipliers, combined signed/unsigned multipliers, and other values of n.

Improved 64-bit Radix-16 Booth Multiplier Based on Partial Product Array Height Reduction

In this paper, we describe an optimization for binary radix-16 (modified) Booth recoded multipliers to reduce the maximum height of the partial product columns to \(\left\lceil \frac{n}{4} \right\rceil\) for unsigned operands. This is in contrast to the conventional maximum height of \(\left\lceil \frac{n+1}{4} \right\rceil\). Therefore, a reduction of one unit in the maximum height is achieved. This reduction may add flexibility during the design of the pipelined multiplier to meet the design goals, it may allow further optimizations of the partial product array reduction stage in terms of area/delay/power and/or may allow additional addends to be included in the partial product array without increasing the delay. The method can be extended to Booth recoded radix-8 multipliers, signed multipliers, combined signed/unsigned multipliers, and other values of n.
Lessons learned from the EU project T-CREST

A three year EU project, such a T-CREST, with partners from all over Europe and with backgrounds from different domains is a challenging endeavor. Successful execution of such a project depends on more factors than simply performing excellent research. Within the three-year project T-CREST eight partners from academia and industry developed and evaluated a time-predictable multi-core processor with an accompanying compiler and a worst-case execution time analysis tool. The tight cooperation of the partners and the shared vision of the need of new computer architectures for future real-time systems enabled the successful completion of the T-CREST project. The T-CREST platform is now available, with most components in open source, to be used for future real-time systems and as a platform for further research.
Authors: Schoeberl, M. (Intern)
Pages: 870-875
Publication date: 2016

Host publication information
Title of host publication: Proceedings of the 2016 Design, Automation and Test in Europe Conference & Exhibition (DATE)
Publisher: IEEE
ISBN (Print): 978-3-9815370-6-2
BFI conference series: Design, Automation, and Test in Europe (5000366)
Main Research Area: Technical/natural sciences
Conference: 19th Conference and Exhibition on Design, Automation and Test in Europe Conference and Exhibition (DATE 2016), Dresden, Germany, 14/03/2016 - 14/03/2016
Links:
http://ieeexplore.ieee.org/xpls/abs_all.jsp?arnumber=7459431
Source: FindIt
Source-ID: 277554487
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Logic and Timing Analysis of Genetic Logic Circuits using D-VASim

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Baig, H. (Intern), Madsen, J. (Intern)
Pages: 77-78
Publication date: 2016

Host publication information
Title of host publication: Proceedings of the 8th International Workshop on Bio-Design Automation (IWBDA 2016)
Main Research Area: Technical/natural sciences
Workshop: 8th International Workshop on Bio-Design Automation, Newcastle upon Tyne, United Kingdom, 16/08/2016 - 16/08/2016
Electronic versions:
IWBDA_2016.pdf
Links:
http://www.iwbdaconf.org/2016/program/
Source: PublicationPreSubmission
Source-ID: 127113795
Publication: Research - peer-review › Conference abstract in proceedings – Annual report year: 2016

Microfluidic Very Large Scale Integration (VLSI): Modeling, Simulation, Testing, Compilation and Physical Synthesis

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Pop, P. (Intern), Minhas, W. H. (Intern), Madsen, J. (Intern)
Number of pages: 270
Publication date: 2016

Publication information
Publisher: Springer
ISBN (Print): 978-3-319-29597-8
ISBN (Electronic): 978-3-319-29599-2
Original language: English
Main Research Area: Technical/natural sciences
DOIs:
10.1007/978-3-319-29599-2
Source: FindIt
Source-ID: 2305217436
Publication: Research - peer-review › Book – Annual report year: 2016

Mind the tracker you wear: a security analysis of wearable health trackers
Wearable tracking devices have gained widespread usage and popularity because of the valuable services they offer, monitoring human's health parameters and, in general, assisting persons to take a better care of themselves.
Nevertheless, the security risks associated with such devices can represent a concern among consumers, because of the sensitive information these devices deal with, like sleeping patterns, eating habits, heart rate and so on. In this paper, we analyse the key security and privacy features of two entry level health trackers from leading vendors (Jawbone and Fitbit), exploring possible attack vectors and vulnerabilities at several system levels. The results of the analysis show how these devices are vulnerable to several attacks (perpetrated with consumer-level devices equipped with just Bluetooth and Wi-Fi) that can compromise users' data privacy and security, and eventually call the tracker vendors to raise the stakes against such attacks.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Goyal, R. (Ekstern), Dragoni, N. (Intern), Spognardi, A. (Intern)
Number of pages: 6
Pages: 131-136
Publication date: 2016

**Host publication information**

Title of host publication: Proceedings of the 31st ACM Symposium on Applied Computing (SAC’16)
Publisher: ACM
ISBN (Print): 978-1-4503-3739-7
BFI conference series: ACM Symposium on Applied Computing (5000292)
Main Research Area: Technical/natural sciences
Privacy, Security, Wearable health trackers

**Model-Based Evaluation Of System Scalability: Bandwidth Analysis For Smartphone-Based Biosensing Applications**

Scalability is a design principle often valued for the engineering of complex systems. Scalability is the ability of a system to change the current value of one of its specification parameters. Although targeted frameworks are available for the evaluation of scalability for specific digital systems, methodologies enabling scalability analysis of multidomain, complex systems, are still missing. In acknowledgment of the importance for complex systems to present the ability to change or evolve, we present in this work a system-level model-based methodology allowing the multidisciplinary parametric evaluation of scalability. Our approach can be used to determine how a set of limited changes to targeted system modules could affect design specifications of interest. It can also help predict and trace system bottlenecks over several product generations, offering system designers the chance to to better plan re-engineering efforts for scaling a system specification efficaciously.

We demonstrate the value of our methodology by investigating a smartphone-based biosensing instrumentation platform. Specifically, we carry out scalability analysis for the system’s bandwidth specification: the maximum analog voltage waveform excitation frequency the system could output while allowing continuous acquisition and wireless streaming of bioimpedance measurements. We rely on several SysML modelling tools, including dependency matrices, as well as a fault-detection Simulink Stateflow executable model to conclude on how the successive re-engineering of 5 independent system modules, from the replacement of a wireless Bluetooth interface, to the revision of the ADC sample-and-hold operation could help increase system bandwidth.

**General information**

State: Published
Organisations: Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Patou, F. (Intern), Madsen, J. (Intern), Dimaki, M. (Intern), Svendsen, W. E. (Intern)
Number of pages: 5
Pages: 718-722
Publication date: 2016

**Host publication information**

Title of host publication: Proceedings of Euromicro Conference on Digital System Design 2016
Publisher: IEEE
ISBN (Electronic): 978-1-5090-2817-7
Main Research Area: Technical/natural sciences
Performance/Power Space Exploration for Binary64 Division Units

The digit-recurrence division algorithm is used in several high-performance processors because it provides good tradeoffs in terms of latency, area and power dissipation. In this work we develop a minimally redundant radix-8 divider for binary64 (double-precision) aiming at obtaining better energy efficiency in the performance-per-watt space. The results show that the radix-8 divider, when compared to radix-4 and radix-16 units, requires less energy to complete a division for high clock rates.
Reconfiguration in FPGA-Based Multi-Core Platforms for Hard Real-Time Applications

In general-purpose computing multi-core platforms, hardware accelerators and reconfiguration are means to improve performance; i.e., the average-case execution time of a software application. In hard real-time systems, such average-case speed-up is not in itself relevant - it is the worst-case execution-time of tasks of an application that determines the systems ability to respond in time. To support this focus, the platform must provide service guarantees for both communication and computation resources. In addition, many hard real-time applications have multiple modes of operation, and each mode has specific requirements. An interesting perspective on reconfigurable computing is to exploit run-time reconfiguration to support mode changes. In this paper we explore approaches to reconfiguration of communication and computation resources in the T-CREST hard real-time multi-core platform. The reconfiguration of communication resources is supported by extending the message-passing network-on-chip with capabilities for setting up, tearing down, and modifying the bandwidth of virtual circuits. The reconfiguration of computation resources, such as hardware accelerators, is performed using the dynamic partial reconfiguration capabilities found in modern FPGAs.
Routing Optimization of AVB Streams in TSN Networks

In this paper we are interested in safety-critical real-time applications implemented on distributed architectures using the Time-Sensitive Networking (TSN) standard. The ongoing standardization of TSN is an IEEE effort to bring deterministic real-time capabilities into the IEEE 802.1 Ethernet standard supporting safety-critical systems and guaranteed Quality-of-Service. TSN will support Time-Triggered (TT) communication based on schedule tables, Audio-Video-Bridging (AVB) streams with bounded end-to-end latency as well as Best-Effort messages. We consider that we know the topology of the network as well as the routes and schedules of the TT streams. We are interested to determine the routing of the AVB streams such that all frames are schedulable and their worst-case end-to-end delay is minimized. We have proposed a search-space reduction technique and a Greedy Randomized Adaptive Search Procedure (GRASP)-based heuristic for this routing optimization problem. The proposed approaches has been evaluated using several test cases.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, TTTech Computertechnik AG
Authors: Laursen, S. M. (Intern), Pop, P. (Intern), Steiner, W. (Ekstern)
Number of pages: 6
Pages: 43-48
Publication date: 2016
Workshop: 14th International Workshop on Real-Time Networks (RTN 2016), Toulouse, France, 05/07/2016 - 05/07/2016
Main Research Area: Technical/natural sciences

Publication information
Journal: ACM SIGBED Review
Volume: 13
Issue number: 4
ISSN (Print): 1551-3688
Original language: English
Electronic versions:
Sune_Molgaard_Laursen2016aa_Routing_Optimization_of_AVB_St_SIGBED_Review_1.pdf
DOIs:
10.1145/3015037.3015044
Source: PublicationPreSubmission
Source-ID: 127146854
Publication: Research - peer-review › Conference article – Annual report year: 2016

SafeDroid: A Distributed Malware Detection Service for Android

Android platform has become a primary target for malware. In this paper we present SafeDroid, an open source distributed service to detect malicious apps on Android by combining static analysis and machine learning techniques. It is composed by three micro-services, working together, combining static analysis and machine learning techniques. SafeDroid has been designed as a user friendly service, providing detailed feedback in case of malware detection. The detection service is optimized to be lightweight and easily updated. The feature set on which the micro-service of detection relies on has been selected and optimized in order to focus only on the most distinguishing characteristics of the Android apps. We present a prototype to show the effectiveness of the detection mechanism service and the feasibility of the approach.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Safety-critical Java for embedded systems

This paper presents the motivation for and outcomes of an engineering research project on certifiable Java for embedded systems. The project supports the upcoming standard for safety-critical Java, which defines a subset of Java and libraries aiming for development of high criticality systems. The outcome of this project includes prototype safety-critical Java implementations, a time-predictable Java processor, analysis tools for memory safety, and example applications to explore the usability of safety-critical Java for this application area. The text summarizes developments and key contributions and concludes with the lessons learned.

Copyright © 2016 John Wiley & Sons, Ltd.
Security And Privacy Issues in Health Monitoring Systems: eCare@Home Case Study

Automated systems for monitoring elderly people in their home are becoming more and more common. Indeed, an increasing number of home sensor networks for healthcare can be found in the recent literature, indicating a clear research direction in smart homes for health-care. Although the huge amount of sensitive data these systems deal with and expose to the external world, security and privacy issues are surprisingly not taken into consideration. The aim of this paper is to raise some key security and privacy issues that home health monitor systems should face with. The analysis is based on a real world monitoring sensor network for healthcare built in the context of the eCare@Home project.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Wearing, T. (Ekstern), Dragoni, N. (Intern)
Number of pages: 6
Publication date: 2016

Host publication information
Title of host publication: Proceedings of the 1st Workshop on Emerging eHealth through Internet of Things (EHIoT 2016)
Main Research Area: Technical/natural sciences
Workshop: 1st Workshop on Emerging eHealth through Internet of Things (EHIoT 2016), Västerås, Sweden, 19/10/2016 - 19/10/2016
Source: PublicationPreSubmission
Source-ID: 2349786218
Publication: Research - peer-review › Journal article – Annual report year: 2016

Smartphone-based biosensing platform evolution: implementation of electrochemical analysis capabilities

Lab-on-Chip technologies offer great opportunities for the democratization of in-vitro medical diagnostics to the consumer-market. Despite the limitations set by the strict instrumentation and control requirements of certain families of these
devices, new solutions are emerging. Smartphones now routinely demonstrate their potential as an interface of choice for operating complex, instrumented Lab-on-Chips. The sporadic nature of home-based in-vitro medical diagnostics testing calls for the development of systems capable of evolving with new applications or new technologies for Lab-on-Chip devices. We present in this work how we evolved the first generation of a smartphone/Lab-on-Chip platform designed for evolvability. We demonstrate how reengineering efforts can be confined to the mobile-software layer and illustrate some of the benefits of building evolvable systems. We implement electrochemical capabilities on our platform prototype and carry out cyclic voltammetry to measure dopamine concentrations over several orders of magnitude.

General information
State: Published
Organisations: Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Department of Electrical Engineering, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Patou, F. (Intern), Dimaki, M. (Intern), Svendsen, W. E. (Intern), Kjærgaard, C. (Intern), Madsen, J. (Intern)
Number of pages: 5
Publication date: 2016

Host publication information
Title of host publication: Proceedings of the 10th International Symposium on Medical Information and Communication Technology (ISMICT)
Publisher: IEEE
ISBN (Electronic): 9781509028498
Main Research Area: Technical/natural sciences
Conference: 10th International Symposium on Medical Information and Communication Technology, Worcester, MA, United States, 20/03/2016 - 20/03/2016
Electronic versions: ISMICT2016_conf_PATOU.pdf
DOIs: 10.1109/ISMICT.2016.7498881
Source: PublicationPreSubmission
Source-ID: 122818729
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

State-based Communication on Time-predictable Multicore Processors
Some real-time systems use a form of task-to-task communication called state-based or sample-based communication that does not impose any flow control among the communicating tasks. The concept is similar to a shared variable, where a reader may read the same value multiple times or may not read a given value at all. This paper explores time-predictable implementations of state-based communication in network-on-chip based multicore platforms through five algorithms. With the presented analysis of the implemented algorithms, the communicating tasks of one core can be scheduled independently of tasks on other cores. Assuming a specific time-predictable multicore processor, we evaluate how the read and write primitives of the five algorithms contribute to the worst-case execution time of the communicating tasks. Each of the five algorithms has specific capabilities that make them suitable for different scenarios.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Sørensen, R. B. (Intern), Schoeberl, M. (Intern), Sparsø, J. (Intern)
Pages: 225-234
Publication date: 2016

Host publication information
Title of host publication: Proceedings of the 24th International Conference on Real-Time Networks and Systems (RTNS ‘16)
Publisher: Association for Computing Machinery
ISBN (Print): 978-1-4503-4787-7
Main Research Area: Technical/natural sciences
Conference: 24th International Conference on Real-Time Networks and Systems, Brest, France, 19/10/2016 - 19/10/2016
Real-time systems, Network-on-chip, Multicore, Message-passing
DOIs: 10.1145/2997465.2997480
Source: PublicationPreSubmission
Source-ID: 127118886
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016
Support for the Logical Execution Time Model on a Time-predictable Multicore Processor

The logical execution time (LET) model increases the compositionality of real-time task sets. Removal or addition of tasks does not influence the communication behavior of other tasks. In this work, we extend a multicore operating system running on a time-predictable multicore processor to support the LET model. For communication between tasks we use message passing on a time-predictable network-on-chip to avoid the bottleneck of shared memory. We report our experiences and present results on the costs in terms of memory and execution time.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Universitat Augsburg
Authors: Kluge, F. (Ekstern), Schoeberl, M. (Intern), Ungerer, T. (Ekstern)
Number of pages: 6
Pages: 61-66
Publication date: 2016
Workshop: 14th International Workshop on Real-Time Networks (RTN 2016), Toulouse, France, 05/07/2016 - 05/07/2016
Main Research Area: Technical/natural sciences

Publication information
Journal: ACM SIGBED Review
Volume: 13
Issue number: 4
ISSN (Print): 1551-3688
Original language: English
Electronic versions:
Support_for_the_Logical_Execution_Time_Model_on_a_postprint.pdf
DOIs: 10.1145/3015037.3015047
Publication: Research - peer-review › Conference article – Annual report year: 2016

Synthesis of Application-Specific Fault-Tolerant Digital Microfluidic Biochip Architectures

Digital microfluidic biochips (DMBs) are microfluidic devices that manipulate droplets on an array of electrodes. Microfluidic operations, such as transport, mixing, and split, are performed on the electrode array to perform a biochemical application. All previous work assumes that the DMB architecture is given and most approaches consider a rectangular shape for the electrode array. However, nonrectangular application-specific architectures are common in practice. Hence, in this paper, we propose an approach to the synthesis of application-specific architectures, such that the cost of the architecture is minimized and the timing constraints of the biochemical application are satisfied. DMBs can be affected by permanent faults, which may lead to the failure of the biochemical application. Our approach introduces redundant electrodes to synthesize fault-tolerant architectures aiming at increasing the yield of DMBs. We have used a tabu search metaheuristic for this architecture synthesis problem. We have proposed a technique to evaluate the architecture alternatives visited during the search, in terms of their impact on the timing constraints of the application. The proposed architecture synthesis approach has been evaluated using several benchmarks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alistar, M. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Number of pages: 14
Pages: 764-777
Publication date: 2016
Main Research Area: Technical/natural sciences

Publication information
Volume: 35
Issue number: 5
ISSN (Print): 0278-0070
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 1.682 SJR 0.485
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 1
Synthesis of railway-signaling plans using reachability games

In this work, we show the feasibility of using functional programming (more specifically F#) in connection with game-based methods for synthesis of correct-by-construction controllers (also called signaling plans) for railway networks. This is a massively resource-demanding application. A model for railway networks comprising trains, signals, linear sections, and points is established together with a domain-specific language capturing the important concepts in the model. A translation from railway network models to two-player reachability games is provided. In these games, the existential player (the control system) controls signals and points and the universal player (the antagonistic environment) controls movement of trains. A winning strategy for the existential player provides a signaling plan that will safely guide trains through the network. The concepts from the railway network model and the two-player reachability game are captured, in a natural manner, by type declarations in F#. Furthermore, the F# translation functions are formulated in a manner that is close to the mathematical formulations. This increases confidence in the correctness of the implementation and it decreases the
development time. Imperative features of F# proved useful in two places: Hash tables and arrays were used in the representations of the railway network model and the reachability game. This allowed for more compact representations and a more efficient game solver (providing the winning strategy). Experiments show that we are able to synthesize signaling plans for real railway networks of substantial size.

**General information**

*State:* Published  
*Organisations:* Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Flow Robotics  
*Authors:* Kasting, P. F. S. (Intern), Hansen, M. R. (Intern), Vester, S. (Ekstern)  
*Number of pages:* 13  
*Publication date:* 2016

**Host publication information**

*Title of host publication:* 28th Symposium on the Implementation and Application of Functional Programming Languages, Volume: Part F127410  
*Publisher:* Association for Computing Machinery  
*ISBN (Print):* 9781450347679

*Series:* Acm Int. Conf. Proc. Ser  
*Main Research Area:* Technical/natural sciences  
*Computer Programming, Computer Programming Languages, Information Sources and Analysis, Applied Mathematics, Computer programming languages, Functions, Problem oriented languages, Railroads, Signaling, Translation (languages), Transportation, Compact representation, Correct-by-construction, Development time, Domain specific languages, Imperative features, Mathematical formulation, Railway signaling, Translation functions, Functional programming  
*Electronic versions:* a9_kasting.pdf  
*DOIs:* 10.1145/3064899.3064908

**TACLeBench: A benchmark collection to support worst-case execution time research**

Engineering related research, such as research on worst-case execution time, uses experimentation to evaluate ideas. For these experiments we need example programs. Furthermore, to make the research experimentation repeatable those programs shall be made publicly available. We collected open-source programs, adapted them to a common coding style, and provide the collection in open-source. The benchmark collection is called TACLeBench and is available from GitHub in version 1.9 at the publication date of this paper. One of the main features of TACLeBench is that all programs are self-contained without any dependencies on standard libraries or an operating system.

**General information**

*State:* Published  
*Organisations:* Embedded Systems Engineering, Department of Applied Mathematics and Computer Science, Hamburg University of Technology, University of Amsterdam, University of Antwerp, Mälardalen University, University of Toulouse, Friedrich-Alexander University Erlangen-Nuremberg, AbsInt Angewandte Informatik GmbH  
*Authors:* Falk, H. (Ekstern), Altmeyer, S. (Ekstern), Hellinckx, P. (Ekstern), Lisper, B. (Ekstern), Puffitsch, W. (Intern), Rochange, C. (Ekstern), Schoeberl, M. (Intern), Sørensen, R. B. (Intern), Wägemann, P. (Ekstern), Wegener, S. (Ekstern)  
*Pages:* 2.1-2.10  
*Publication date:* 2016  
*Main Research Area:* Technical/natural sciences

**Publication information**

*Journal:* Open Access Series in Informatics  
*Volume:* 55  
*ISSN (Print):* 2190-6807  
*Ratings:*  
*ISI indexed (2013):* ISI indexed no  
*ISI indexed (2012):* ISI indexed no  
*ISI indexed (2011):* ISI indexed no  
*Original language:* English  
*Geography, Planning and Development, Modeling and Simulation, Benchmark, Real-time systems, WCET analysis, Benchmarking, Interactive computer systems, Open source projects, Open sources, Standard libraries, Wcet analysis, Worst-case execution time, Real time systems
The Personal Health Technology Design Space

Interest is increasing in personal health technologies that utilize mobile platforms for improved health and well-being. However, although a wide variety of these systems exist, each is designed quite differently and materializes many different and more or less explicit design assumptions. To enable designers to make informed and well-articulated design decisions, the authors propose a design space for personal health technologies. This space consists of 10 dimensions related to the design of data sampling strategies, visualization and feedback approaches, treatment models, and regulatory constraints.

General Information

State: Published
Organisations: Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, IT University of Copenhagen
Authors: Bardram, J. E. (Intern), Frost, M. (Ekstern)
Pages: 70-78
Publication date: 2016
Main Research Area: Technical/natural sciences

Publication Information

Journal: IEEE Pervasive Computing
Volume: 15
Issue number: 2
ISSN (Print): 1536-1268
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 1.122 SJR 0.326
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 1
Scopus rating (2016): SJR 0.471 SNIP 1.407 CiteScore 2.59
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.52 SNIP 1.911 CiteScore 2.31
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.609 SNIP 2.648 CiteScore 2.88
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.762 SNIP 3.015 CiteScore 3.01
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.615 SNIP 2.935 CiteScore 3.09
BFI (2011): BFI-level 1
Scopus rating (2011): SJR 0.905 SNIP 4.222 CiteScore 3.89
BFI (2010): BFI-level 1
Scopus rating (2010): SJR 0.746 SNIP 3.528
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.989 SNIP 4.032
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 1.082 SNIP 3.782
Scopus rating (2006): SJR 1.208 SNIP 4.598
Scopus rating (2005): SJR 1.647 SNIP 5.46
Scopus rating (2004): SJR 1.454 SNIP 8.643
The SafeCOP ECSEL Project: Safe Cooperating Cyber-Physical Systems Using Wireless Communication

This paper presents an overview of the ECSEL project entitled "Safe Cooperating Cyber-Physical Systems using Wireless Communication" (SafeCOP), which runs during the period 2016 -- 2019. SafeCOP targets safety-related Cooperating Cyber-Physical Systems (CO-CPS) characterised by use of wireless communication, multiple stakeholders, dynamic system definitions (openness), and unpredictable operating environments. SafeCOP will provide an approach to the safety assurance of CO-CPS, enabling thus their certification and development. The project will define a runtime manager architecture for runtime detection of abnormal behaviour, triggering if needed a safe degraded mode. SafeCOP will also develop methods and tools, which will be used to produce safety assurance evidence needed to certify cooperative functions. SafeCOP will extend current wireless technologies to ensure safe and secure cooperation. SafeCOP will also contribute to new standards and regulations, by providing certification authorities and standardization committees with the scientifically validated solutions needed to craft effective standards extended to also address cooperation and system-of-systems issues. The project has 28 partners from 6 European countries, and a budget of about 11 million Euros corresponding to about 1,300 person-months.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Alten Sverige AB, Mälardalen University
Authors: Pop, P. (Intern), Scholle, D. (Ekstern), Hansson, H. (Ekstern), Widforss, G. (Ekstern), Rosqvist, M. (Ekstern)
Number of pages: 7
Pages: 532-538
Publication date: 2016

Host publication information
Title of host publication: Proceedings of Euromicro Conference on Digital System Design 2016
Publisher: IEEE
ISBN (Electronic): 978-1-5090-2817-7
Main Research Area: Technical/natural sciences
Wireless communication, Cyber-physical systems, Systems-of-systems, Safety-assurance

Electronic versions:
The_SafeCOP_ECSEL_Project_postprint.pdf
DOIs:
10.1109/DSD.2016.25
Source: FindIt
Source-ID: 2347976327
Publication: Research - peer-review › Article in proceedings – Annual report year: 2016

Time-Predictable Communication on a Time-Division Multiplexing Network-on-Chip Multicore

This thesis presents time-predictable inter-core communication on a multicore platform with a time-division multiplexing (TDM) network-on-chip (NoC) for hard real-time systems. The thesis is structured as a collection of papers that contribute within the areas of: reconfigurable TDM NoCs, static TDM scheduling, and time-predictable inter-core communication. More specifically, the work presented in this thesis investigates the interaction between hardware and software involved in time-predictable inter-core communication on the multicore platform. The thesis presents: a new generation of the Argo NoC network interface (NI) that supports instantaneous reconfiguration, a TDM traffic scheduler that generates virtual circuit (VC) configurations for the Argo NoC, and software functions for two types of intercore communication.

The new generation of the Argo NoC adds the capability of instantaneously reconfiguring VCs and it addresses the identified shortcomings of the previous generation. The VCs provide the guaranteed bandwidth and latency required to implement time-predictable inter-core communication on top of the Argo NoC. This new Argo generation is, in terms of hardware, less than half the size of NoCs that provide similar functionalities and it offers a higher degree of flexibility to the application programmer.
The developed TDM scheduler supports a generic TDM NoC and custom parameterizable communication patterns. These communication patterns allow the application programmer to generate schedules that provide a set of VCs that efficiently uses the hardware resources. The TDM scheduler also shows better results, in terms of TDM period, compared to previous state-of-the-art TDM schedulers. Furthermore, we provide a description of how a communication pattern can be optimized in terms of shortening the TDM period.

The thesis identifies two types of inter-core communication that are commonly used in real-time systems: message passing and state-based communication. We implement message passing as a circular buffer with the data transfer through the NoC. The worst-case execution time (WCET) of the send and receive functions of our implementation is not dependent on the message size. We also implement five algorithms for state-based communication and analyze them in terms of the WCET and worst-case communication delay. The five algorithms each have scenarios where they are better than the others.

This thesis shows in detail how time-predictable inter-core communication can be implemented in an efficient way, from the low-level hardware to the high-level software functions.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Sørensen, R. B. (Intern), Sparsø, J. (Intern), Schoeberl, M. (Intern)
Number of pages: 143
Publication date: 2016

Publication information
Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English
Series: DTU Compute PHD-2016
Number: 423
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions:
phd423_Sorensen_RB.pdf

Relations
Projects:
Time-Predictable Communication on a Time-Division Multiplexing Network-on-Chip Multicore
Publication: Research › Ph.D. thesis – Annual report year: 2016

Time-predictable Stack Caching
Embedded systems are computing systems for controlling and interacting with physical environments. Embedded systems with special timing constraints where the system needs to meet deadlines are referred to as real-time systems. In hard real-time systems, missing a deadline causes the system to fail completely. Thus, in systems with hard deadlines the worst-case execution time (WCET) of the real-time software running on them needs to be bounded.

Modern architectures use features such as pipelining and caches for improving the average performance. These features, however, make the WCET analysis more complicated and less imprecise. Time-predictable computer architectures provide solutions to this problem. As accesses to the data in caches are one source of timing unpredictability, devising methods for improving the timepredictability of caches are important. Stack data, with statically analyzable addresses, provides an opportunity to predict and tighten the WCET of accesses to data in caches.

In this thesis, we introduce the time-predictable stack cache design and implementation within a time-predictable processor. We introduce several optimizations to our design for tightening the WCET while keeping the timepredictability of the design intact. Moreover, we provide a solution for reducing the cost of context switching in a system using the stack cache. In design of these caches, we use custom hardware and compiler support for delivering time-predictable stack data accesses. Furthermore, for systems where compiler support or hardware changes are not practical, we propose and explore two different alternatives based on only software and only hardware support.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Abbaspourseyedi, S. (Intern), Schoeberl, M. (Intern), Sparsø, J. (Intern)
Number of pages: 133
Time-Predictable Virtual Memory

Virtual memory is an important feature of modern computer architectures. For hard real-time systems, memory protection is a particularly interesting feature of virtual memory. However, current memory management units are not designed for time-predictability and therefore cannot be used in such systems. This paper investigates the requirements on virtual memory from the perspective of hard real-time systems and presents the design of a time-predictable memory management unit. Our evaluation shows that the proposed design can be implemented efficiently. The design allows address translation and address range checking in constant time of two clock cycles on a cache miss. This constant time is in strong contrast to the possible cost of a miss in a translation look-aside buffer in traditional virtual memory organizations. Compared to a platform without a memory management unit, these two additional clock cycles per cache miss introduce only a small performance overhead.

Timing Analysis of Genetic Logic Circuits using D-VASim

A genetic logic circuit is a gene regulator network implemented by re-engineering the DNA of a cell, in order to control gene expression or metabolic pathways, through a logic combination of external signals, such as chemicals or proteins. As for electronic logic circuits, timing and propagation delay analysis may play a very significant role in the designing of genetic logic circuits. In this demonstration, we present the capability of D-VASim (Dynamic Virtual Analyzer and Simulator) to perform the timing and propagation delay analysis of genetic logic circuits. Using D-VASim, the timing and propagation delay analysis of single as well as cascaded genetic logic circuits can be performed. D-VASim allows user to change the circuit parameters during runtime simulation to observe its effect on circuit's timing behavior. The results obtained from D-VASim can be used not only to characterize the timing behavior of genetic logic circuits but also to analyze the timing constraints of cascaded genetic logic circuits.
Towards Unifying OpenMP Under the Task-Parallel Paradigm Implementation and Performance of the taskloop Construct

OpenMP 4.5 introduced a task-parallel version of the classical thread-parallel for-loop construct: the taskloop construct. With this new construct, programmers are given the opportunity to choose between the two parallel paradigms to parallelize their for loops. However, it is unclear where and when the two approaches should be used when writing efficient parallel applications. In this paper, we explore the taskloop construct. We study performance differences between traditional thread-parallel for loops and the new taskloop directive. We introduce an efficient implementation and compare our implementation to other taskloop implementations using micro-and kernel-benchmarks, as well as an application. We show that our taskloop implementation on average results in a 3.2% increase in peak performance when compared against corresponding parallel-for loops.

Traffic class assignment for mixed-criticality frames in TTEthernet

In this paper we are interested in mixed-criticality applications, which have functions with different timing requirements, i.e., hard real-time (HRT), soft real-time (SRT) and functions that are not time-critical (NC). The applications are implemented on distributed architectures that use the TTEthernet protocol for communication. TTEthernet supports three traffic classes: Time-Triggered (TT), where frames are transmitted based on static schedule tables; Rate Constrained (RC), for dynamic frames with a guaranteed bandwidth and bounded delays; and Best Effort (BE), for which no timing guarantees are provided. HRT messages have deadlines, whereas for SRT messages we capture the quality-of-service using "utility functions". Given the network topology, the set of application messages and their routing, we are interested to determine the traffic class of each message, such that all HRT messages are schedulable and the total utility for SRT messages is maximized. For the TT frames we decide their schedule tables, and for the RC frames we decide their bandwidth allocation. We propose a Tabu Search-based metaheuristic to solve this optimization problem. The proposed approach has been evaluated using several benchmarks, including two realistic test cases.
Voice analysis as an objective state marker in bipolar disorder

Changes in speech have been suggested as sensitive and valid measures of depression and mania in bipolar disorder. The present study aimed at investigating (1) voice features collected during phone calls as objective markers of affective states in bipolar disorder and (2) if combining voice features with automatically generated objective smartphone data on behavioral activities (for example, number of text messages and phone calls per day) and electronic self-monitored data (mood) on illness activity would increase the accuracy as a marker of affective states. Using smartphones, voice features, automatically generated objective smartphone data on behavioral activities and electronic self-monitored data were collected from 28 outpatients with bipolar disorder in naturalistic settings on a daily basis during a period of 12 weeks. Depressive and manic symptoms were assessed using the Hamilton Depression Rating Scale 17-item and the Young Mania Rating Scale, respectively, by a researcher blinded to smartphone data. Data were analyzed using random forest algorithms. Affective states were classified using voice features extracted during everyday life phone calls. Voice features were found to be more accurate, sensitive and specific in the classification of manic or mixed states with an area under the curve (AUC)=0.89 compared with an AUC=0.78 for the classification of depressive states. Combining voice features with automatically generated objective smartphone data on behavioral activities and electronic self-monitored data increased the accuracy, sensitivity and specificity of classification of affective states slightly. Voice features collected in naturalistic settings using smartphones may be used as objective state markers in patients with bipolar disorder.
Voice analysis as an objective state marker in bipolar disorder

General information
State: Published
Organisations: Copenhagen Center for Health Technology, Department of Applied Mathematics and Computer Science, Cognitive Systems, Embedded Systems Engineering, Copenhagen University Hospital, Rigshospitalet, IT University of Copenhagen
Authors: Faurholt-Jepsen, M. (Ekstern), Busk, J. (Ekstern), Frost, M. (Ekstern), Vinberg, M. (Ekstern), Christensen, E. M. (Ekstern), Winther, O. (Intern), Bardram, J. E. (Intern), Kessing, L. V. (Ekstern)
Number of pages: 1
Pages: 103
Publication date: 2016
Conference: 18th Annual Conference of the International Society for Bipolar Disorders (ISBD 2016), Amsterdam, Netherlands, 13/07/2016 - 13/07/2016
Main Research Area: Technical/natural sciences

Publication information
Journal: Bipolar Disorders (English Edition, Online)
Volume: 18
Issue number: Supplement S1
ISSN (Print): 1399-5618
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 1.355 SJR 2.354
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 4.35 SJR 2.481 SNIP 1.325
Scopus rating (2015): SJR 2.558 SNIP 1.488 CiteScore 4.68
Web of Science (2015): Indexed yes
Scopus rating (2014): SJR 3.286 SNIP 1.732 CiteScore 4.94
Scopus rating (2013): SJR 2.618 SNIP 1.509 CiteScore 4.8
Scopus rating (2012): SJR 3.084 SNIP 1.753 CiteScore 5.42
Scopus rating (2011): SJR 2.743 SNIP 1.625 CiteScore 4.84
Scopus rating (2010): SJR 2.711 SNIP 1.474
Scopus rating (2009): SJR 3.041 SNIP 1.566
Scopus rating (2008): SJR 2.764 SNIP 1.218
Scopus rating (2007): SJR 2.834 SNIP 1.368
Scopus rating (2006): SJR 2.228 SNIP 1.328
Scopus rating (2005): SJR 2.283 SNIP 1.128
Scopus rating (2004): SJR 2.23 SNIP 1.262
Scopus rating (2003): SJR 2.197 SNIP 0.988
Scopus rating (2002): SJR 2.48 SNIP 0.836
Scopus rating (2001): SJR 0.789 SNIP 0.653
Why Hackers Love eHealth Applications
The tsunami of Internet-of-Things and mobile applications for healthcare is giving hackers an easy way to burrow deeper into our lives as never before. In this paper we argue that this security disaster is mainly due to a lack of consideration by the healthcare IT industry in security and privacy issues. By means of a representative healthcare mobile app, we analyse the main vulnerabilities that eHealth applications should deal with in order to protect user data and related privacy.

Adaptive Multipath Key Reinforcement for Energy Harvesting Wireless Sensor Networks
Energy Harvesting - Wireless Sensor Networks (EH-WSNs) constitute systems of networked sensing nodes that are capable of extracting energy from the environment and that use the harvested energy to operate in a sustainable state. Sustainability, seen as design goal, has a significant impact on the design of the security protocols for such networks, as the nodes have to adapt and optimize their behaviour according to the available energy. Traditional key management schemes do not take energy into account, making them not suitable for EH-WSNs. In this paper we propose a new multipath key reinforcement scheme specifically designed for EH-WSNs. The proposed scheme allows each node to take into consideration and adapt to the amount of energy available in the system. In particular, we present two approaches, one static and one fully dynamic, and we discuss some experimental results.

Energy Harvesting Wireless Sensor Networks (EH-WSNs) represent an interesting new paradigm where individual nodes forming a network are powered by energy sources scavenged from the surrounding environment. This technique provides numerous advantages, but also new design challenges. Securing the communications under energy constraints represents one of these key challenges. The amount of energy available is theoretically infinite in the long run but highly variable over short periods of time, and managing it is a crucial aspect. In this paper we present an adaptive approach for security in multihop EH-WSNs which allows different nodes to dynamically choose the most appropriate energy-affecting parameters such as encryption algorithm and key size, providing in this way energy savings. In order to provide evidence of the approach’s feasibility in a real-world network, we have designed and implemented it as extension of on-demand medium access control (ODMAC), a receiver-initiated (RI) MAC protocol specifically designed and developed to address the foundational energy-related needs of Energy Harvesting Wireless Sensor Networks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Department of Informatics and Mathematical Modeling, Embedded Systems Engineering, University of Bristol, Örebro University
Authors: Di Mauro, A. (Intern), Fafoutis, X. (Ekstern), Dragoni, N. (Intern)
Number of pages: 11
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication information
Journal: International Journal of Distributed Sensor Networks
Volume: 2015
Article number: 760302
ISSN (Print): 1550-1329
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 0.745 SJR 0.255
A Framework and Classification for Fault Detection Approaches in Wireless Sensor Networks with an Energy Efficiency Perspective

Wireless Sensor Networks (WSNs) are more and more considered a key enabling technology for the realisation of the Internet of Things (IoT) vision. With the long term goal of designing fault-tolerant IoT systems, this paper proposes a fault detection framework for WSNs with the perspective of energy efficiency to facilitate the design of fault detection methods and the evaluation of their energy efficiency. Following the same design principle of the fault detection framework, the paper proposes a classification for fault detection approaches. The classification is applied to a number of fault detection approaches for the comparison of several characteristics, namely, energy efficiency, correlation model, evaluation method, and detection accuracy. The design guidelines given in this paper aim at providing an insight into better design of energy-efficient detection approaches in resource-constraint WSNs.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, East China Normal University
Authors: Zhang, Y. (Ekstern), Dragoni, N. (Intern), Wang, J. (Ekstern)
Number of pages: 11
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication information
Journal: International Journal of Distributed Sensor Networks
Volume: 2015
Article number: 678029
ISSN (Print): 1550-1329
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 0.745 SJR 0.255
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 1.16 SJR 0.256 SNIP 0.727
Scopus rating (2015): SJR 0.256 SNIP 0.877 CiteScore 1.1
Web of Science (2015): Indexed yes
Scopus rating (2014): SJR 0.242 SNIP 0.699 CiteScore 0.85
Web of Science (2014): Indexed yes
Scopus rating (2013): SJR 0.231 SNIP 0.899 CiteScore 1.13
Scopus rating (2012): SJR 0.192 SNIP 0.586 CiteScore 0.87
Scopus rating (2011): SJR 0.16 SNIP 0.44 CiteScore 0.53
Scopus rating (2010): SJR 0.146 SNIP 0.237
Scopus rating (2009): SJR 0.303 SNIP 0.78
Web of Science (2009): Indexed yes
Scopus rating (2008): SJR 0.287 SNIP 0.919
Scopus rating (2007): SJR 0.193 SNIP 1.045

Original language: English
COMPUTER, TELECOMMUNICATIONS, BLOCK CIPHER, PROTOCOLS
Electronic versions:
760302.pdf
DOIs:
10.1155/2015/760302
Source: FindIt
Source-ID: 275106193
Publication: Research - peer-review › Journal article – Annual report year: 2015
An approach to multicore parallelism using functional programming: A case study based on Presburger Arithmetic

In this paper we investigate multicore parallelism in the context of functional programming by means of two quantifier-elimination procedures for Presburger Arithmetic: one is based on Cooper’s algorithm and the other is based on the Omega Test.

We first develop correct-by-construction prototype implementations in a functional programming language. Thereafter, the parallelism inherent in the decision procedures is analyzed using the Directed Acyclic Graph (DAG) model of multicore parallelism. In the step from a DAG model to a parallel implementation, the parallel implementation is optimized taking into account negative factors such as cache misses, garbage collection and overhead due to task creations, because such factors may introduce sequential bottlenecks with severe consequences for the parallel efficiency.

The experiments were conducted using the functional programming language F# and .NET platform executing on an 8-core machine. A speedup of approximately 4 was obtained for Cooper’s algorithm and a speedup of approximately 6 was obtained for the exact-shadow part of the Omega Test.

The considered procedures are complex, memory-intense algorithms on huge formula trees and the case study reveals more general applicable techniques and guideline for deriving parallel algorithms from sequential ones in the context of data-intensive tree algorithms. The obtained insights should apply for any strict and impure functional programming language.

Furthermore, the results obtained for the exact-shadow elimination procedure have a wider applicability because they can directly be transferred to the Fourier–Motzkin elimination method.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Dung, P. A. (Intern), Hansen, M. R. (Intern)
Number of pages: 17
Pages: 2–18
Publication date: 2015
BFI conference series: Nordic Workshop on Programming Theory (5010899)
Main Research Area: Technical/natural sciences

Publication information
Journal: Journal of Logic and Algebraic Programming
Volume: 84
Issue number: 1
ISSN (Print): 1567-8326
Ratings:
BFI (2018): BFI-level 2
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 0 SJR 0.106
BFI (2016): BFI-level 2
Scopus rating (2016): SJR 0.402 SNIP 1.197
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.678 SNIP 2.742 CiteScore 1.55
An Asynchronous Time-Division-Multiplexed Network-on-Chip for Real-Time Systems

Multi-processor architectures using networks-on-chip (NOCs) for communication are becoming the standard approach in the development of embedded systems and general purpose platforms. Typically, multi-processor platforms follow a globally asynchronous locally synchronous (GALS) timing organization. This thesis focuses on the design of Argo, a NOC targeted at hard real-time multi-processor platforms with a GALS timing organization.

To support real-time communication, NOCs establish end-to-end connections and provide latency and throughput guarantees for these connections. Argo uses time division multiplexing (TDM) in combination with a static schedule to implement virtual end-to-end circuits. TDM is a straightforward way to provide guarantees and to share the resources efficiently, and it has an efficient hardware implementation. Argo supports a GALS system organization, and additionally it explores more flexible timing within its structure, to address signal distribution issues, using a network of synchronous routers.

NOCs consist of a switching structure of routers connected by links, with network interfaces (NIs) that connect the processors to the switching structure. Argo uses a novel NI design that supports time-predictability, and asynchronous routers that form a time-elastic network. The NI design integrates the DMA functionality and the TDM schedule, and uses dual-ported local memories. The routers combine the router functionality and asynchronous elastic behavior. They also use a gating mechanism to reduce the energy consumption. The combination of the NI design and the router design supports the formation of end-to-end paths in the NOC, from the local memory of a sending core to the local memory of a receiving core. These end-to-end paths do not require any dynamic arbitration, buffering, flow control, or clock synchronization, in the routers or the NIs.
This thesis explores the implementation of the individual components of Argo, as well as several complete instances of the Argo NOC. The implementations target both FPGA technology and 65 nm CMOS technology. It is shown that (i) the NI design is scalable and four to five times smaller than previously published NIs for similar NOCs, (ii) the router design is power efficient and two to three times smaller than equivalent router designs, and (iii) the overall Argo NOC is around four times smaller than other TDM NOCs. Argo is an important part of the T-CREST platform and used in a number of configurations.

The flexible timing organization of Argo combines asynchronous routers with mesochronous NIs, which are connected to individually clocked cores, supporting a GALS system organization. The mesochronous NIs operate at the same frequency, possibly with some skew, while the network of asynchronous routers absorbs this skew within certain limits. The elasticity of the asynchronous network is explored, answering the question of how much skew the Argo NOC can absorb. A qualitative analysis studies the parameters affecting the elasticity and its limits. A quantitative analysis models the Argo behavior using timed-graph models and worst-case timing separation of events analysis to evaluate the elasticity of Argo. The results show that the skew absorbed by the network of routers can be two or more cycles, depending on the frequency applied at its endpoints, the NIs.

Overall this thesis presents the design and implementation of Argo, and the analysis of its elastic behavior. It shows that Argo provides hard real-time guarantees in a straightforward way, it has an efficient implementation and it is time-elastic.
A Scalable Prescriptive Parallel Debugging Model

Debugging is a critical step in the development of any parallel program. However, the traditional interactive debugging model, where users manually step through code and inspect their application, does not scale well even for current supercomputers due its centralized nature. While lightweight debugging models, which have been proposed as an alternative, scale well, they can currently only debug a subset of bug classes. We therefore propose a new model, which we call prescriptive debugging, to fill this gap between these two approaches. This user-guided model allows programmers to express and test their debugging intuition in a way that helps to reduce the error space. Based on this debugging model we introduce a prototype implementation embodying this model, the DySectAPI, allowing programmers to construct probe trees for automatic, event-driven debugging at scale. In this paper we introduce the concepts behind DySectAPI and, using both experimental results and analytical modelling, we show that the DySectAPI implementation can run with a low overhead on current systems. We achieve a logarithmic scaling of the prototype and show predictions that even for a large system the overhead of the prescriptive debugging model will be small.

A Smart Mobile Lab-on-Chip-Based Medical Diagnostics System Architecture Designed For Evolvability

Unprecedented knowledge levels in life sciences along with technological advances in micro- and nanotechnologies and microfluidics have recently conditioned the advent of Lab-on-Chip (LoC) devices for In-Vitro Medical Testing (IVMT). Combined with smart-mobile technologies, LoCs are pervasively giving rise to opportunities to better diagnose disease, predict and monitor personalised treatment efficacy, or provide healthcare decision-making support at the Point-of-Care (PoC). Although made increasingly available to the consumer market, the adoption of LoC-based PoC In-Vitro Medical Testing (IVMT) systems is still in its infancy. This attrition partly pertains to the intricacy of designing and developing complex systems, destined to be used sporadically, in a fast-pace evolving technological paradigm. System evolvability is therefore key in the design process and constitutes the main motivation for this work.

We introduce a smart-mobile and LoC-based system architecture designed for evolvability. By propagating LoC programmability, instrumentation, and control tools to the highlevel abstraction smart-mobile software layer, our architecture facilitates the realisation of new use-cases and the accommodation for incremental LoC-technology developments. We demonstrate these features with an implementation allowing the interfacing of LoCs embedding current- or impedance-
based biosensors such as Silicon Nanowire Field Effect Transistors (SiNW-FETs) or electrochemical transducers. Structural modifications of these LoCs or changes in their specific operation may be addressed by the sole reengineering of the mobile software layer, minimizing system upgrade development and validation costs and efforts.

**General information**

State: Published
Organisations: Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Center for Bachelor of Engineering Studies, Afdelingen for Elektronik, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Patou, F. (Intern), Dimaki, M. (Intern), Svendsen, W. E. (Intern), Kjaergaard, C. (Intern), Madsen, J. (Intern)
Pages: 390-398
Publication date: 2015

**Host publication information**

Title of host publication: Proceedings of the Euromicro Conference on Digital System Design 2015
Publisher: IEEE
ISBN (Print): 9781467380355
BFI conference series: Euromicro Symposium on Digital Systems Design (5000380)
Main Research Area: Technical/natural sciences
Lab-on-Chip, Smartphone, Point-of-care, In-vitro medical diagnostics, System evolvability, System architecting
Electronic versions:
Certified_DSD2015_paper.pdf
DOIs:
10.1109/DSD.2015.11
Source: PublicationPreSubmission
Source-ID: 115264502
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

**A Time-Composable Operating System for the Patmos Processor**

In the last couple of decades we have witnessed a steady growth in the complexity and widespread of real-time systems. In order to master the rising complexity in the timing behaviour of those systems, rightful attention has been given to the development of time-predictable computer architectures. The Patmos time-predictable microprocessor used in the T-CREST project employs performance-enhancing hardware while keeping the system analyzable. Time composability, at both hardware and software level, is a considerable aid to reducing the integration costs of complex applications. A time-composable operating system, on top of a time-composable processor, facilitates incremental development, which is highly desirable for industry. This paper makes a twofold contribution. First, we present enhancements to the Patmos processor to allow achieving time composability at the operating system level. Second, we extend an existing time-composable operating system, TiCOS, to make best use of advanced Patmos hardware features in the pursuit of time composability.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Padua
Authors: Ziccardi, M. (Ekstern), Schoeberl, M. (Intern), Vardanega, T. (Ekstern)
Pages: 1892-1897
Publication date: 2015

**Host publication information**

Title of host publication: Proceedings of the 30th Annual ACM Symposium on Applied Computing (SAC ‘15)
Publisher: Association for Computing Machinery
ISBN (Print): 978-1-4503-3196-8
BFI conference series: ACM Symposium on Applied Computing (5000292)
Main Research Area: Technical/natural sciences
Conference: 30th Annual ACM/SIGAPP Symposium on Applied Computing, Salamanca, Spain, 13/04/2015 - 13/04/2015
Real-time Operating System, Time Composability, Time Predictability
DOIs:
10.1145/2695664.2695685
Source: PublicationPreSubmission
Source-ID: 118552874
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015
Attributes Enhanced Role-Based Access Control Model

Attribute-based access control (ABAC) and role-based access control (RBAC) are currently the two most popular access control models. Yet, they both have known limitations and offer features complementary to each other. Due to this fact, integration of RBAC and ABAC has recently emerged as an important area of research. In this paper, we propose an access control model that combines the two models in a novel way in order to unify their benefits. Our approach provides a fine-grained access control mechanism that not only takes contextual information into account while making the access control decisions but is also suitable for applications where access to resources is controlled by exploiting contents of the resources in the policy.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Texas
Authors: Mahmood Rajpoot, Q. (Intern), Jensen, C. D. (Intern), Krishnan, R. (Ekstern)
Pages: 3-17
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 12th International Conference on Trust, Privacy and Security in Digital Business (TrustBus’15)
Publisher: Springer
Editors: Fischer-Huebner, S., Lambrinoudakis, C.
ISBN (Print): 978-3-319-22905-8
ISBN (Electronic): 978-3-319-22906-5
Series: Lecture Notes in Computer Science
Volume: 9264
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
Conference: 12th International Conference on Trust, Privacy and Security in Digital Business (TrustBus’15), Valencia, Spain, 01/09/2015 - 01/09/2015
Context-aware access control, RBAC, Attributes, Content-based access control, Role-permission explosion, Role-explosion
Electronic versions:
AERBAC_TrustBus_20150618_.pdf
DOIs:
10.1007/978-3-319-22906-5_1
Source: PublicationPreSubmission
Source-ID: 110979339
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Characterization of RNS multiply-add units for power efficient DSP

In the past decades, the Residue Number System (RNS) has been adopted in DSP as an alternative to the traditional two's complement number system (TCS) because of the savings in area, higher speed and reduced power dissipation. In this work, we perform a comprehensive Design Space Exploration (DSE) for a fused multiply-add unit by taking into account four metrics: area, delay, power consumption, and switching activity. The results of the DSE are verified against the TCS and RNS implementation of parallel FIR filters of different characteristics. In both the DSE and the filter implementation, we consider two design corners: maximum speed and minimum area. The experimental results demonstrate that for high data rates and high order filters, the RNS implementation is more power efficient than the TCS because of the reduced switching activity and the larger amount of low-power cells placed in the unit.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Roma ‘Tor Vergata'
Authors: Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Petricca, M. (Ekstern), Re, M. (Ekstern)
Number of pages: 4
Publication date: 2015

Host publication information
Title of host publication: Conference Proceedings of the 58th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2015) : "Climbing to New Heights"
Publisher: IEEE
ISBN (Print): 978-1-4673-6557-4
Main Research Area: Technical/natural sciences
Continuous Context-Aware Device Comfort Evaluation Method

Mobile devices have become more powerful and are increasingly integrated in the everyday life of people; from playing games, taking pictures and interacting with social media to replacing credit cards in payment solutions. The security of a mobile device is therefore increasingly linked to its context, such as its location, surroundings (e.g. objects and people in the immediate environment) and so on, because some actions may only be appropriate in some situations; this is not captured by traditional security models. In this paper, we examine the notion of Device Comfort and propose a way to calculate the sensitivity of a specific action to the context. We present two different methods for a mobile device to dynamically evaluate its security status when an action is requested, either by the user or by another device. The first method uses the predefined ideal context as a standard to assess the comfort level of a device in the current context. The second method is based on the familiarity of the device with doing the particular action in the current context. These two methods suit different situations of the device owner's ability to deal with system security. The assessment result can activate responding action of the device to protect its resource.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Xidian University
Authors: Guo, J. (Ekstern), Jensen, C. D. (Intern), Ma, J. (Ekstern)
Pages: 203-211
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 9th IFIP WG 11.11 International Conference on Trust Management IX (IFIPTM 2015)
Publisher: Springer
Editors: Jensen, C. D., Marsh, S., Dimitrakos, T., Murayama, Y.
ISBN (Print): 978-3-319-18490-6
ISBN (Electronic): 978-3-319-18491-3

Series: IFIP AICT - Advances in Information and Communication technology
Number: 454
ISSN: 1868-4238
Main Research Area: Technical/natural sciences
Conference: 9th IFIP WG 11.11 International Conference on Trust Management, Hamburg, Germany, 26/05/2015 - 26/05/2015
Context-aware, Device comfort, Mobile device

Continuous-flow biochips: Current platforms and emerging research challenges: Special Session

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, National Chiao Tung University, University of California, Duke University
Authors: Pop, P. (Intern), Ho, T. (Ekstern), Chakrabarty, K. (Ekstern), Grover, W. H. (Ekstern)
Pages: 24-27
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 28th International Conference on VLSI Design: Held concurrently with the 14th International Conference on Embedded Systems
Publisher: IEEE Computer Society Press
Continuous-Flow Biochips: Technology, Physical Design Methods and Testing

This article is a tutorial on continuous-flow biochips where the basic building blocks are microchannels, and microvalves, and by combining them, more complex units such as mixers, switches, and multiplexers can be built. It also presents the state of the art in flow-based biochip technology and emerging research challenges in the areas of physical design and testing techniques.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Stanford University, Duke University
Authors: Pop, P. (Intern), Araci, I. E. (Ekstern), Chakrabarty, K. (Ekstern)
Pages: 8-19
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication information
Journal: IEEE Design & Test
Volume: 32
Issue number: 6
ISSN (Print): 2168-2356
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 0.91 SJR 0.273
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 1.13 SJR 0.271 SNIP 1.11
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.323 SNIP 1.085 CiteScore 1
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.383 SNIP 1.235 CiteScore 0.76
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 0.564 SNIP 1.681
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.771 SNIP 2.336
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.525 SNIP 1.458
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.586 SNIP 1.504
BFI (2009): BFI-level 2
Scopus rating (2009): SJR 0.502 SNIP 1.651
BFI (2008): BFI-level 2
Scopus rating (2008): SJR 0.783 SNIP 2.49
Scopus rating (2007): SJR 0.711 SNIP 1.994
Scopus rating (2006): SJR 0.473 SNIP 1.638
Scopus rating (2005): SJR 0.658 SNIP 1.674
Design of Mixed-Criticality Applications on Distributed Real-Time Systems

A mixed-criticality system implements applications of different safety-criticality levels onto the same platform. In such cases, the certification standards require that applications of different criticality levels are protected so they cannot influence each other. Otherwise, all tasks have to be developed and certified according to the highest criticality level, dramatically increasing the development costs. In this thesis we consider mixed-criticality real-time applications implemented on distributed partitioned architectures.

Partitioned architectures use temporal and spatial separation mechanisms to ensure that applications of different criticality levels do not interfere with each other. With temporal partitioning, each application is allowed to run only within predefined time slots, allocated on each processor. The sequence of time slots for all the applications on a processor are grouped within a Major Frame, which is repeated periodically. Each partition can have its own scheduling policy; we have considered non-preemptive static cyclic scheduling and fixed-priority preemptive scheduling policies. We assume that the communication network implements the TTEthernet protocol, which supports Time-Triggered (TT) messages transmitted based on static schedule tables, Rate Constrained (RC) messages with bounded end-to-end delay, and Best-Effort (BE) messages, for which no timing guarantees are provided. TTEthernet offers spatial separation for mixed-criticality messages through the concept of virtual links, and temporal separation, enforced through schedule tables for TT messages and bandwidth allocation for RC messages.

The objective of this thesis is to develop methods and tools for distributed mixed-criticality real-time systems. At the processor level, we are interested to determine (i) the mapping of tasks to processors, (ii) the assignment of tasks to partitions, (iii) the decomposition of tasks into redundant lower criticality tasks, (iv) the sequence and size of the partition time slots on each processor and (v) the schedule tables, such that all the applications are schedulable and the development and certification costs are minimized. We have proposed Simulated Annealing and Tabu Search metaheuristics to solve these optimization problems. The proposed algorithms have been evaluated using several benchmarks.

At the communication network level, we are interested in the design optimization of TTEthernet networks used to transmit mixed-criticality messages. Given the set of TT and RC messages, and the topology of the network, we are interested to optimize (i) the packing of messages in frames, (ii) the assignment of frames to virtual links, (iii) the routing of virtual links and (iv) the TT static schedules, such that all frames are schedulable and the worst-case end-to-end delay of the RC messages is minimized. We have proposed a Tabu Search-based metaheuristic for this optimization problem.

The proposed algorithm has been evaluated using several benchmarks. The optimization approaches have also been evaluated using realistic aerospace case studies. In this context, we have shown how to extend the proposed optimization frameworks to also take into account quality of service constraints. For TTEthernet networks, we have also proposed a topology selection method to reduce the cost of the architecture.
In this article, we are interested in implementing mixed-criticality real-time embedded applications on a given heterogeneous distributed architecture. Applications have different criticality levels, captured by their Safety-Integrity Level (SIL), and are scheduled using static-cyclic scheduling. According to certification standards, mixed-criticality tasks can be integrated onto the same architecture only if there is enough spatial and temporal separation among them. We consider that the separation is provided by partitioning, such that applications run in separate partitions, and each partition is allocated several time slots on a processor. Tasks of different SILs can share a partition only if they are all elevated to the highest SIL among them. Such elevation leads to increased development costs, which increase dramatically with each SIL. Tasks of higher SILs can be decomposed into redundant structures of lower SIL tasks. We are interested to determine (i) the mapping of tasks to processors, (ii) the assignment of tasks to partitions, (iii) the decomposition of tasks into redundant lower SIL tasks, (iv) the sequence and size of the partition time slots on each processor, and (v) the schedule tables, such that all the applications are schedulable and the development costs are minimized. We have proposed a Tabu Search-based approach to solve this optimization problem. The proposed algorithm has been evaluated using several synthetic and real-life benchmarks.
Design optimization of TTEthernet-based distributed real-time systems

Many safety-critical real-time applications are implemented using distributed architectures, composed of heterogeneous processing elements interconnected in a network. Our focus in this paper is on the TTEthernet protocol, a deterministic, synchronized and congestion-free network protocol based on the Ethernet standard and compliant with the ARINC 664 Specification Part 7. TTEthernet is highly suitable for safety-critical real-time applications since it offers separation for messages using the concept of virtual links and supports three time-criticality classes: Time-Triggered (TT), Rate-Constrained (RC) and Best-Effort. In this paper we are interested in the design optimization of TTEthernet networks used to transmit real-time application messages. Given the set of TT and RC messages, and the topology of the network, our approach optimizes the packing of messages in frames, the assignment of frames to virtual links, the routing of virtual links and the TT static schedules, such that all frames are schedulable and the worst-case end-to-end delay of the RC messages is minimized. We propose a Tabu Search-based metaheuristic for this optimization problem. The proposed algorithm has been evaluated using several benchmarks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, TTTech Computertechnik AG
Authors: Tamas-Selicean, D. (Intern), Pop, P. (Intern), Steiner, W. (Ekstern)
Number of pages: 35
Pages: 1-35
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication Information
Journal: Real-Time Systems
Volume: 51
Issue number: 1
ISSN (Print): 0922-6443
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 2.237 SJR 0.257
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 2.26 SJR 0.392 SNIP 1.703
Developing merged CDIO based curricula for diploma (B.Eng.) IT study programs at DTU

Starting 2007, the Danish government drew up a new map of universities through a process of mergers of a number of universities and research institutions (UFM 2007), as part of the national innovation strategy. In the beginning of 2013, the Engineering College Copenhagen (IHK, now DTU Ballerup) merged with the Technical University of Denmark (DTU Lyngby). The goal of the merger was to educate ever more innovative diploma engineers to fulfill the needs by Danish industry through combining a practice-oriented development environment and a research-oriented environment.

Merging a university with an engineering college implies merging two different cultures: established teaching staff, different study lines; a difficult undertaking at best. Existing study lines must be merged, overlaps and differences identified and handled, and in general a common understanding and language must be established.

The two institutions represented before the merger well 3500 B.Eng. students. The goal of the merger was to combine the best of the existing educations rooted in a practice-oriented development environment and a research-oriented environment. At the same time, the merger was supposed to contribute to the national innovation strategy.

In this paper we describe the process of developing new, merged B.Eng curricula in the IT field (Diploma IT), as part of the merger between DTU Lyngby and IHK. Particular attention will be given to the following subjects:
• The design process used to develop the new merged study programs;
• Involvement of stakeholders in designing the new curricula;
• Introduction of a common interdisciplinary innovation course in the programs; and
• Education of teaching staff: Integration into one organization.

General information
State: Published
Authors: Nyborg, M. (Intern), Probst, C. W. (Intern), Stassen, F. (Intern)
Number of pages: 12
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 11th International CDIO Conference
Publisher: CDIO
Main Research Area: Technical/natural sciences
Conference: 11th International CDIO Conference, Chengdu, China, 08/06/2015 - 08/06/2015
CDIO-based study programs, Stakeholder involvement, Innovation
Electronic versions:
CDIO2015_final.pdf
Links:
http://www.cdio.org/node/5996 (Link to full proceedings)
Source: PublicationPreSubmission
Source-ID: 118017742
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

D-VASim: Dynamic Virtual Analyzer and Simulator for Genetic Circuits
A genetic circuit represents a gene regulator network that is triggered by a combination of external signals, such as chemicals, proteins, light or temperature, to emit signals to control gene expression or metabolic pathways accordingly. In order to match the intended behaviour, genetic circuits are either assembled from a standard library of well-defined genetic gates or from parts of an available library, for instance, BioBricks. The obtained behavior can be validated through in-silico analysis, solving reaction kinetics using ordinary differential equations (ODEs) or by stochastic simulation, with the aim to reduce the number of required in-vitro experiments.

We present a behavioural simulation and analysis tool that allows the biologist to carry out virtual lab experiments as an interactive process during simulation of the genetic circuit, rather than a batch process, which is current practice. We believe that this increases the insights gained from the analysis and allows for exploring more parameters in an intuitive manner.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Copenhagen Center for Health Technology
Authors: Baig, H. (Intern), Madsen, J. (Intern)
Pages: 48-49
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 7th International Workshop on Bio-Design Automation (IWBDA 2015)
Main Research Area: Technical/natural sciences
Conference: 7th International Workshop on Bio-Design Automation, Seattle, United States, 19/08/2015 - 19/08/2015
Electronic versions:
D_VASim_Camera_ready_Hasan_and_Jan_.pdf
Links:
http://www.iwbdaconf.org/2015/program/#proceedings (Link to proceedings at the conference web-site)
Source: PublicationPreSubmission
Source-ID: 118030132
Publication: Research - peer-review › Conference abstract in proceedings – Annual report year: 2015

Efficient Context Switching for the Stack Cache: Implementation and Analysis
The design of tailored hardware has proven a successful strategy to reduce the timing analysis overhead for (hard) real-time systems. The stack cache is an example of such a design that has been proven to provide good average-case performance, while being easy to analyze.
So far, however, the analysis of the stack cache was limited to individual tasks, ignoring aspects related to multitasking. A major drawback of the original stack cache design is that, due to its simplicity, it cannot hold the data of multiple tasks at the same time. Consequently, the entire cache content needs to be saved and restored when a task is preempted.

We propose (a) an analysis exploiting the simplicity of the stack cache to bound the overhead induced by task pre-emption and (b) an extension of the design that allows to (partially) hide the overhead by virtualizing stack caches.


Fault-tolerant event detection is fundamental to wireless sensor network applications. Existing approaches usually adopt neighborhood collaboration for better detection accuracy, while need more energy consumption due to communication. Focusing on energy efficiency, this paper makes an improvement to a hybrid algorithm for dynamic event region detection, such as real-time tracking of chemical leakage regions. Considering the characteristics of the moving away dynamic events, we propose a return back condition for the hybrid algorithm from distributed neighborhood collaboration, in which a node makes its detection decision based on decisions received from its spatial and temporal neighbors, to local non-communicative decision making. The simulation results demonstrate that the improved algorithm does not degrade the detection accuracy of the original algorithm, while it has better energy efficiency with the number of messages exchanged in the network decreased.


Fault-tolerant event detection is fundamental to wireless sensor network applications. Existing approaches usually adopt neighborhood collaboration for better detection accuracy, while need more energy consumption due to communication. Focusing on energy efficiency, this paper makes an improvement to a hybrid algorithm for dynamic event region detection, such as real-time tracking of chemical leakage regions. Considering the characteristics of the moving away dynamic events, we propose a return back condition for the hybrid algorithm from distributed neighborhood collaboration, in which a node makes its detection decision based on decisions received from its spatial and temporal neighbors, to local non-communicative decision making. The simulation results demonstrate that the improved algorithm does not degrade the detection accuracy of the original algorithm, while it has better energy efficiency with the number of messages exchanged in the network decreased.
Experiences with Compiler Support for Processors with Exposed Pipelines

Field programmable gate arrays, FPGAs, have become an attractive implementation technology for a broad range of computing systems. We recently proposed a processor architecture, Tinuso, which achieves high performance by moving complexity from hardware to the compiler tool chain. This means that the compiler tool chain must handle the increased complexity. However, it is not clear if current production compilers can successfully meet the strict constraints on instruction order and generate efficient object code. In this paper, we present our experiences developing a compiler backend using the GNU Compiler Collection, GCC. For a set of C benchmarks, we show that a Tinuso implementation with our GCC backend reaches a relative speedup of up to 1.73 over a similar Xilinx Micro Blaze configuration while using 30% fewer hardware resources. While our experiences are generally positive, we expose some limitations in GCC that need to be addressed to achieve the full performance potential of Tinuso.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Language-Based Technology, Embedded Systems Engineering
Authors: Jensen, N. B. (Intern), Schleuniger, P. (Intern), Hindborg, A. E. (Intern), Walter, M. (Intern), Karlsson, S. (Intern)
Pages: 137-143
Publication date: 2015

Fame for sale: Efficient detection of fake Twitter followers
Fake followers are those Twitter accounts specifically created to inflate the number of followers of a target account. Fake followers are dangerous for the social platform and beyond, since they may alter concepts like popularity and influence in the Twittersphere - hence impacting on economy, politics, and society. In this paper, we contribute along different dimensions. First, we review some of the most relevant existing features and rules (proposed by Academia and Media) for anomalous Twitter accounts detection. Second, we create a baseline dataset of verified human and fake follower accounts. Such baseline dataset is publicly available to the scientific community. Then, we exploit the baseline dataset to train a set of machine-learning classifiers built over the reviewed rules and features. Our results show that most of the rules proposed by Media provide unsatisfactory performance in revealing fake followers, while features proposed in the past by Academia for spam detection provide good results. Building on the most promising features, we revise the classifiers both in terms of reduction of overfitting and cost for gathering the data needed to compute the features. The final result is a novel Class A classifier, general enough to thwart overfitting, lightweight thanks to the usage of the less costly features, and still able to correctly classify more than 95% of the accounts of the original training set. We ultimately perform an information fusion-based sensitivity analysis, to assess the global sensitivity of each of the features employed by the classifier. The findings reported in this paper, other than being supported by a thorough experimental methodology and interesting on their own, also pave the way for further investigation on the novel issue of fake Twitter followers.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, IIT-CNR, Bell Labs
Authors: Cresci, S. (Ekstern), Di Pietro, R. (Ekstern), Petrocchi, M. (Ekstern), Spognardi, A. (Intern), Tesconi, M. (Ekstern)
Pages: 56-71
Publication date: 2015
Main Research Area: Technical/natural sciences
Fault Detection in WSNs - An Energy Efficiency Perspective Towards Human-Centric WSNs

Energy efficiency is a key factor to prolong the lifetime of wireless sensor networks (WSNs). This is particularly true in the design of human-centric wireless sensor networks (HCWSN) where sensors are more and more embedded and they have to work in resource-constraint settings. Resource limitation has a significant impact on the design of a WSN and the adopted fault detection method. This paper investigates a number of fault detection approaches and proposes a fault detection framework based on an energy efficiency perspective. The analysis and design guidelines given in this paper aims at representing a first step towards the design of energy-efficient detection approaches in resource-constraint WSN, like HCWSNs.
Fault-Tolerant Digital Microfluidic Biochips: Compilation and Synthesis

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark, East China Normal University, Örebro University
Authors: Orfanidis, C. (Ekstern), Zhang, Y. (Ekstern), Dragoni, N. (Intern)
Pages: 285-300
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 9th KES International Conference on Agent and Multi-Agent Systems: Technologies and Applications (KES-AMSTA 2015)
Publisher: Springer
Editors: Jezic, G., Howlett, R. J., Jain, L. C.
ISBN (Print): 978-3-319-19727-2
ISBN (Electronic): 78-3-319-19728-9
Series: Smart Innovation, Systems and Technologies
Volume: 38
BFI conference series: International Conference on Agent and Multi-Agent Systems: Technology and Applications (5000019)
Main Research Area: Technical/natural sciences
Conference: 9th International KES International Conference on Agent and Multi-Agent Systems: Technologies and Applications (KES-AMSTA 2015), Sorrento, Italy, 17/06/2015 - 17/06/2015
DOIs:
10.1007/978-3-319-19728-9_24
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Fault-Tolerant Topology Selection for TTEthernet Networks

Many safety-critical real-time applications are implemented using distributed architectures, composed of heterogeneous processing elements (PEs) interconnected in a network. In this paper, we are interested in the TTEthernet protocol, which is a deterministic, synchronized and congestion-free network protocol based on the IEEE 802.3 Ethernet standard and compliant with ARINC 664p7. TTEthernet supports three types of traffic: static time-triggered (TT) traffic and dynamic traffic, which is further subdivided into Rate Constrained (RC) traffic that has bounded end-to-end latencies, and Best-Effort (BE) traffic, for which no timing guarantees are provided. TTEthernet offers spatial separation through the concept of virtual links (VLs), and temporal separation, through schedule tables for TT messages and bandwidth allocation for RC messages. Given a set of PEs, we are interested to determine a fault-tolerant network topology, consisting of redundant physical links and network switches, such that the architecture cost is minimized, the applications are fault-tolerant to a given number of permanent faults occurring in the communication network, and the timing constraints of the TT and RC messages are satisfied. Deciding on a fault-tolerant topology means (i) deciding on the number of network switches, (ii) the physical links and the network topology, (iii) the routing of VLs on top of the physical network, (iv) the assignment of frames to VLs and (v) the schedule tables for the TT frames. We propose a Simulated Annealing meta-heuristic to solve this optimization problem. The proposed approach has been evaluated using a synthetic benchmark and a space case study, based on the Orion Crew Exploration Vehicle.
Fernando: An educational ahead-of-time bytecode compiler

While modern Java virtual machines are efficient and portable, they are also very complex software artifacts. Adapting or extending such a complex system within the scope of a university course is hardly an option. Fernando is a minimalist ahead-of-time bytecode compiler with the aim of providing an educational platform. This paper presents the design of Fernando and explains the reasoning behind various design decisions. The design results in an extremely small code base of around 3k lines of code. While high performance was not a primary design goal, our evaluation shows that Fernando achieves a reasonable level of performance.

Flow-Based Biochips: Fault-Tolerant Design and Error Recovery

The focus of this paper is on continuous-flow biochips, where the basic building block is a microvalve. By combining these microvalves, more complex units such as mixers, switches, multiplexers can be built, hence the name of the technology, “microfluidic Very Large Scale Integration” (mVLSI). Biochips are currently being designed manually using tools such as AutoCAD. Physical defects can be introduced during the fabrication process, which reduces the yield, and may lead to the failure of the biochemical application. Failure is costly because of the need to redo lengthy experiments, using expensive reagents and often hard-to-obtain samples, and can be safety critical (endangering human life), e.g., for important diagnostic procedures (screening for cancer). Researchers have started to propose fault models and test techniques for mVLSI biochips. To increase the yield, and to potentially also prevent the failure during the operation of the biochip, we advocate the use of fault-tolerant biochip design. The vision is to provide application fault-tolerance at run-time (online), detecting the faults as they appear, and reconfiguring the application. However, in this paper our assumption is that the faults are detected during testing, and that the operation of the biochip is reconfigured offline (at design time) to avoid the faults. We are interested to introduce redundancy such that the applications can still successfully run on a defective biochip. Redundancy is the addition of extra resources, normally not needed for correct operation, to be used for fault-
Hardware Locks with Priority Ceiling Emulation for a Java Chip-Multiprocessor

According to the safety-critical Java specification, priority ceiling emulation is a requirement for implementations, as it has preferable properties, such as avoiding priority inversion and being deadlock free on uni-core systems. In this paper we explore our hardware supported implementation of priority ceiling emulation on the multicore Java optimized processor, and compare it to the existing hardware locks on the Java optimized processor. We find that the additional overhead for priority ceiling emulation on a multicore processor is several times higher than simpler, non-preemptive locks, mainly due to slow access to shared memory. We also find that PCE is mostly viable with large critical sections.

Hardware Transactional Memory Optimization Guidelines, Applied to Ordered Maps

Synchronization of concurrent data structures is difficult to get right. Fine-grained synchronization locks small data chunks, but requires too high an overhead per chunk, traditional coarse-grained synchronization locks big data chunks, and thereby makes them unavailable to other threads. Neither synchronization method scales well. Recently, hardware transactional memory was introduced, which allows threads to use transactions instead of locks. So far, applying hardware transactional memory has shown mixed results. We believe this is because transactions are different from locks, and using them efficiently requires reasoning about those differences. In this paper we present 5 guidelines for applying hardware transactional memory efficiently, and apply the guidelines to BT-trees, a concurrent ordered map. Evaluating BT-trees on standard benchmarks shows that they are up to 5.3 times faster than traditional maps using hardware transactional memory, and up to 3.9 times faster than state of the art concurrent ordered maps.
Implementation of an Ethernet-Based Communication Channel for the Patmos Processor

The Patmos processor, which is used as the intellectual property of the T-CREST platform, is only equipped with a RS-232 serial port for communication with the outside world. The serial port is a minimal input/output device with a limited speed and without native networking features. An Ethernet 10/100BASE-T IEEE 802.3 based communication channel is a reliable and high speed communication interface (10/100 Mbits/s) that also supports networking. This technical report presents an implementation of an Ethernet-based communication channel for the Patmos processor, targeting the Terasic DE2-115 development board. We have designed the hardware to interface the EthMac Ethernet controller from OpenCores to Patmos and to the physical chip of the development board, and we have implemented a software library to drive the controller and to support some essential protocols. The design was implemented on an Altera Cyclone IV FPGA in the aforementioned board, and it was tested with a software application, running on Patmos, that uses the Ethernet communication channel while the system is connected to a small local area network.

Integrating Attributes into Role-Based Access Control

Role-based access control (RBAC) and attribute-based access control (ABAC) are currently the most prominent access control models. However, they both suffer from limitations and have features complimentary to each other. Due to this fact, integration of RBAC and ABAC has become a hot area of research recently. We propose an access control model that combines the two models in a novel way in order to unify their benefits. Our approach provides a fine-grained access control mechanism that takes into account the current contextual information while making the access control decisions.
Interfacing Hardware Accelerators to a Time-Division Multiplexing Network-on-Chip

This paper addresses the integration of stateless hardware accelerators into time-predictable multi-core platforms based on time-division multiplexing networks-on-chip. Stateless hardware accelerators, like floating-point units, are typically attached as co-processors to individual processors in the platform. Our design takes a different approach and connects the hardware accelerators to the network-on-chip in the same way as processor cores. Each processor that uses a hardware accelerator is assigned a virtual channel for sending instructions to the hardware accelerator and a virtual channel for receiving results. This allows a stateless and possibly pipelined hardware accelerator to be shared in an interleaved fashion without any form of reservation, and this opens for interesting area-performance trade-offs. The design is developed with a focus on time-predictability, areaefficiency, and FPGA implementation. The design evaluation is carried out using the open source T-CREST multi-core platform implemented on an Altera Cyclone IV FPGA. The size of the proposed design, including a floating-point accelerator, is about two-thirds of a processor.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Pezzarossa, L. (Intern), Sørensen, R. B. (Intern), Schoeberl, M. (Intern), Sparso, J. (Intern)
Number of pages: 4
Publication date: 2015

Introduction
This chapter presents an introduction to the microfluidics field and microfluidic biochips. We discuss the main fluid propulsion principles used by modern microfluidic platforms, with a focus on "digital" microfluidic biochips, which are the topic of this book. Digital microfluidic biochips manipulate the fluids as small "droplets" using electrokinetics, i.e., electrowetting-on-dielectric. Several application areas for biochips are discussed, and the motivation behind the work presented in this book is introduced. At the end of the chapter, we outline the structure of the book and an overview of the topics covered.
Message Passing on a Time-predictable Multicore Processor

Real-time systems need time-predictable computing platforms. For a multicore processor to be time-predictable, communication between processor cores needs to be time-predictable as well. This paper presents a time-predictable message-passing library for such a platform. We show how to build up abstraction layers from a simple, time-division multiplexed hardware push channel. We develop these time-predictable abstractions and implement them in software. To prove the time-predictability of these functions we analyze their worst-case execution time (WCET) with the aiT WCET analysis tool. We combine these WCET numbers with the calculation of the network latency of a message and then provide a statically computed end-to-end latency for this core-to-core message.

Microfluidic very large-scale integration for biochips: Technology, testing and fault-tolerant design

Microfluidic biochips are replacing the conventional biochemical analyzers by integrating all the necessary functions for biochemical analysis using microfluidics. Biochips are used in many application areas, such as, in vitro diagnostics, drug discovery, biotech and ecology. The focus of this paper is on continuous-flow biochips, where the basic building block is a microvalve. By combining these microvalves, more complex units such as mixers, switches, multiplexers can be built, hence the name of the technology, "microfluidic Very Large-Scale Integration" (mVLSI). A roadblock in the deployment of microfluidic biochips is their low reliability and lack of test techniques to screen defective devices before they are used for biochemical analysis. Defective chips lead to repetition of experiments, which is undesirable due to high reagent cost and limited availability of samples. This paper presents the state-of-the-art in the mVLSI platforms and emerging research challenges in the area of continuous-flow microfluidics, focusing on testing techniques and fault-tolerant design.
Modelling and Analysis for Cyber-Physical Systems: An SMT-based approach

This thesis focuses on high-level modelling and analysis of Cyber-Physical Systems (CPS). The rationale is that: since modelling and analysis phases are closely related to the design phase, having better modelling and analysis techniques would tremendously increase quality of designs. Moreover, better designs have positive impacts on the product quality, development time and price, etc.

We developed tools, theories and techniques that make use of SMT solving as a back-end engine for analysis and employ Duration Calculus as a front-end technology for modelling. The proposed techniques have been validated via a few interesting case studies.

In particular, a combination of techniques including reduction to SMT solving, novel simplification for quantified formulas in Linear Integer Arithmetic and multicore parallelism has been used to make Duration Calculus feasible for practical use. Duration Calculus has shown its potential as a domain specific language in a Smart Meter case study. Moreover, counting semantics has proven useful in connection with tool-based support for Duration Calculus.

To extend SMT techniques towards better support for analysis of CPS, we proposed algorithms for handling quantifier alternations and implemented SMT-based optimization procedures. The optimization procedures, available as an extension to Z3 SMT solver, have been instrumental to provide solutions for our case studies in a natural way.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering
Authors: Dung, P. A. (Intern), Hansen, M. R. (Intern)
Number of pages: 83
Publication date: 2015

Models of Communication for Multicore Processors

To efficiently use multicore processors we need to ensure that almost all data communication stays on chip, i.e., the bits moved between tasks executing on different processor cores do not leave the chip. Different forms of on-chip communication are supported by different hardware mechanism, e.g., shared caches with cache coherency protocols, core-to-core networks-on-chip, and shared scratchpad memories. In this paper we explore the different hardware mechanism for on-chip communication and how they support or favor different models of communication. Furthermore, we discuss the usability of the different models of communication for real-time systems.

General information
State: Published
Multithreaded Priority Ceiling Emulation for Safety-Critical Java

Priority ceiling emulation has desirable properties on uniprocessor systems, such as avoiding priority inversion and being deadlock free. This has made it a popular locking protocol. According to the safety-critical Java specification, priority ceiling emulation is a requirement for implementations. However, implementing the protocol for multiprocessor systems is more complex so implementations might perform worse than non-preemptive implementations. In this paper we compare two multiprocessor lock implementations with hardware support for the Java optimized processor: non-preemptive locking and priority ceiling emulation. For the evaluation we analyze the worst-case execution time of the locking routines. We also analyze a safety critical use case with each implementation. We find that the additional software steps necessary for managing priorities in priority ceiling emulation increase the number of locking cycles by at least a factor 15, mainly due to memory contention in a multiprocessor system. This overhead results in the use case being unschedulable using priority ceiling emulation. Any benefits of priority ceiling emulation are also lost when the tasks are completely distributed among the processor. Therefore, given distributed tasks with short critical sections, non-preemptive locking is preferred.

Safety-Critical Java

The Multi-Lane Spatial Logic MLSL introduced by Hilscher et al. in [4] is a two-dimensional spatial logic geared towards modelling and analysis of traffic situations, where the two dimensions are interpreted as the lanes of a road and the distance travelled down that road, respectively. The intended use of MLSL is for capturing (and reasoning about) guards and invariants in decision-making schemes for highly automated driving [12]. Unfortunately, the logic turns out to be undecidable [7,8,11], rendering implementability and thus the actual use of such guard conditions in real-time decision making questionable in general. We here show that under a reasonable model of technical observation of the traffic situation, the actual decidability and implementability issues take a much more pleasing form: given that an actual autonomous car can only sample state information of a finite set of environmental cars in real-time, we show that it is decidable whether truth of an arbitrary MLSL formula can be safely determined on a given sample size. For such feasible formulas, we furthermore state a procedure for determining their truth values based on such a sample.
This paper presents an approach to execute safety-critical applications on multi- and many-core processors in a predictable manner. We investigate three concrete platforms: the Intel Single-chip Cloud Computer, the Texas Instruments TMS320C6678 and the Tilera TILEmpower-Gx36. We define an execution model to safely execute dependent periodic task sets on these platforms. The four rules of the execution model entail that an off-line mapping of the application to the platform must be computed. The paper details our approach to automatically compute a valid mapping. Furthermore, we evaluate our approach, which is based on constraint programming, by applying it to several task sets that are derived from industrial applications.

Given the continuous advancements in the technology of energy harvesting over the last few years, we are now starting to see wireless sensor networks (WSNs) powered by scavenged energy. This change in paradigm has major repercussions not only on the hardware engineering aspects, but also on the software side. The first protocols specifically designed to take advantage of the energy harvesting capabilities of a network have just recently appeared. At the same time, security remains one of the central points of WSNs development, because of their intrinsically unreliable nature that combines a readily accessible communication infrastructure such as wireless data exchange, to an often likewise readily accessible physical deployment. This dissertation provides a comprehensive look at how security can be improved by what energy harvesting has to offer. The main question asked is whether or not it is possible to provide better security in a WSN, by being aware of the fact that the amount of available energy is not going to monotonically decrease over time. The work covers different aspects and components of a WSN and focuses on what is arguably one the most important ones, medium access control (MAC) protocols. An energy-harvesting specific MAC protocol is introduced together with a related security suite. A new attack relevant to a whole class of MAC protocols is also introduced, along with a scheme that defeats it. A security approach for MAC protocols is discussed to provide an energy-aware solution. In order to address security bootstrapping, a new energy-adaptive key reinforcement scheme is presented. Finally an implementation and some experimental results are provided.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Di Mauro, A. (Intern), Dragoni, N. (Intern)
Number of pages: 144
Publication date: 2015
Optimal Scheduling of Stochastic Production Processes Through Model Checking

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering,
Department of Management Engineering, Management Science
Authors: Herbert, L. T. (Intern), Hansen, Z. N. L. (Intern), Sharp, R. (Intern), Jacobsen, P. (Intern)
Pages: 187-202
Publication date: 2015

Host publication information
Title of host publication: Modelling and Management of Engineering Processes : Proceedings of the 3rd International Conference 2013
Publisher: Springer
Editors: Schabacker, M., Gericke, K., Szélig, N., Vajna, S.
ISBN (Print): 978-3-662-44008-7
ISBN (Electronic): 978-3-662-44009-4
Main Research Area: Technical/natural sciences
Publication: Research - peer-review › Book chapter – Annual report year: 2014

Persistence-Based Branch Misprediction Bounds for WCET Analysis
Branch prediction is an important feature of pipelined processors to achieve high performance. However, it can lead to overly pessimistic worst-case execution time (WCET) bounds when being modeled too conservatively. This paper presents bounds on the number of branch mispredictions for local dynamic branch predictors. To handle interferences between branch instructions we use the notion of persistence, a concept that is also found in cache analyses. The bounds apply to branches in general, not only to branches that close a loop. Furthermore, the bounds can be easily integrated into integer linear programming formulations of the WCET problem. An evaluation on a number of benchmarks shows that with these bounds, dynamic branch prediction does not necessarily lead to higher WCET bounds than static prediction schemes.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Puffitsch, W. (Intern)
Pages: 1898-1905
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 30th Annual ACM Symposium on Applied Computing (SAC ’15)
Publisher: Association for Computing Machinery
ISBN (Print): 978-1-4503-3196-8
BFI conference series: ACM Symposium on Applied Computing (5000292)
Main Research Area: Technical/natural sciences
Conference: 30th Annual ACM/SIGAPP Symposium on Applied Computing, Salamanca, Spain, 13/04/2015 - 13/04/2015
Worst-case execution time analysis, Branch prediction
DOIs: 10.1145/2695664.2695728
Source: PublicationPreSubmission
Source-ID: 118024653
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015
Physical trust-based persistent authentication

Recently companies have applied two-factor user authentication. Persistent Authentication is one of the interesting authentication mechanisms to establish security and usability of two-factor authentication systems. However, there is room to improve its feasibility and usability. In this paper, we propose a new type of persistent authentication, called Persistent Authentication Based On physical Trust (PABOT). PABOT uses a context of "physical trust relationship" that is built by visual contact between users, and thus can offer a persistent authentication mechanism with better usability and higher feasibility.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Shizuoka University
Authors: Fujita, M. (Ekstern), Jensen, C. D. (Intern), Arimura, S. (Ekstern), Ikeya, Y. (Ekstern), Nishigaki, M. (Ekstern)
Pages: 186-190
Publication date: 2015

Pin count-aware biochemical application compilation for mVLSI biochips

Microfluidic biochips are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. In this paper we are interested in flow-based biochips, in which the fluidic flow manipulated using integrated microvalves, which are controlled from external pressure sources, connected to "control pins". By combining several microvalves, more complex units, such as micropumps, switches, mixers, and multiplexers, can be built. The current practice is to design these biochips by hand in drawing tools such as AutoCAD, and to program them manually by individually controlling each valve. Recent research has proposed top-down physical synthesis Computer- Aided Design tools, and programming languages and compilation techniques to automatically derive the control signals for the valve actuations. However, researchers have so far assumed that the number of ports used to drive the valves (control pins) is unlimited, which has resulted in very expensive, bulky and energy consuming off-chip control and infeasible control routes in the biochip control layer. In this paper, we propose a methodology to reduce the number of control pins required to run a biochemical application. We focus on the compilation task, where the strategy is to delay operations, without missing their deadlines, such that the sharing of control signals is maximized. The evaluation shows a significant reduction in the number of control pins required.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Lander Raagaard, M. (Ekstern), Pop, P. (Intern)
Pages: 1-6
Publication date: 2015
Power and thermal efficient numerical processing
Numerical processing is at the core of applications in many areas ranging from scientific and engineering calculations to financial computing. These applications are usually executed on large servers or supercomputers to exploit their high speed, high level of parallelism and high bandwidth to memory.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Oticon A/S
Authors: Liu, W. (Intern), Nannarelli, A. (Intern)
Pages: 263-286
Publication date: 2015

Host publication information
Title of host publication: Handbook on Data Centers: Part 1
Publisher: Springer
Editors: Khan, S. U., Zomaya, A. Y.
ISBN (Print): 978-1-4939-2091-4
ISBN (Electronic): 978-1-4939-2092-1
Main Research Area: Technical/natural sciences
DOIs: 10.1007/978-1-4939-2092-1_8
Source: FindIt
Source-ID: 2289019544
Publication: Research - peer-review › Book chapter – Annual report year: 2015

Quantifying system safety: A comparison of the SBOAT & Safety Barrier Manager tools
This paper presents two software tools for analyzing safety risks, SBOAT (Stochastic BPMN Optimisation and Analysis Tool) and SBM (SafetyBarrierManager). SBOAT employs principles from stochastic model checking to allow for the quantitative verification of workflows. SBM supports the creation of valid safety-barrier diagrams and allows the quantitative analysis of the probability of all possible end states of the barrier diagram, i.e. the outcomes if one or several of the barriers fail to perform their barrier function. We compare the foundations of these tools and describe how they can be used and how they complement each other by means of the analysis of a production workflow inspired by a real-world industry case.

General information
State: Published
Organisations: Department of Management Engineering, Management Science, Production and Service Management, Engineering Systems Group, Risk Research Group, Implementation and Performance Management, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Hansen, Z. N. L. (Intern), Duijm, N. J. (Intern), Markert, F. (Intern), Herbert, L. T. (Intern)
Number of pages: 8
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the European Safety and Reliability Conference (ESREL) 2015
Main Research Area: Technical/natural sciences
Conference: 25th European Safety and Reliability Conference (ESREL 2015), Zürich, Switzerland, 07/09/2015 - 07/09/2015
Electronic versions:
Quantifying_system_safety.pdf
Source: PublicationPreSubmission
Source-ID: 110657294
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Receiver-initiated medium access control protocols for wireless sensor networks
One of the fundamental building blocks of a Wireless Sensor Network (WSN) is the Medium Access Control (MAC) protocol, that part of the system governing when and how two independent neighboring nodes activate their respective transceivers to directly interact. Historically, data exchange has always been initiated by the node willing to relay data, i.e. the sender. However, the Receiver-Initiated paradigm introduced by Lin et al. in 2004 with RICER and made popular by Sun et al. in 2008 with RI-MAC, has spawned a whole new stream of research, yielding tens of new MAC protocols. Within such paradigm, the receiver is the one in charge of starting a direct communication with an eligible sender. This allows for new useful properties to be satisfied, novel schemes to be introduced and new challenges to be tackled. In this paper, we present a survey comprising of all the MAC protocols released since the year 2004 that fall under the receiver-initiated category. In particular, keeping in mind the key challenges that receiver-initiated MAC protocols are meant to deal with, we analyze and discuss the different protocols according to common features and design goals. The aim of this paper is to
provide a comprehensive and self-contained introduction to the fundamentals of the receiver-initiated paradigm, providing newcomers with a quick-start guide on the state of the art of this field and a palette of options, essential for implementing applications or designing new protocols.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Fafoutis, X. (Intern), Di Mauro, A. (Intern), Vithanage, M. D. (Ekstern), Dragoni, N. (Intern)
Pages: 55-74
Publication date: 2015
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Computer Networks
Volume: 76
ISSN (Print): 1389-1286
Ratings:
- BFI (2018): BFI-level 2
- Web of Science (2018): Indexed yes
- BFI (2017): BFI-level 2
- Scopus rating (2017): SNIP 1.551 SJR 0.5
- Web of Science (2017): Indexed yes
- BFI (2016): BFI-level 2
- Scopus rating (2016): SJR 0.556 SNIP 1.705 CiteScore 3.26
- BFI (2015): BFI-level 2
- Scopus rating (2015): SJR 0.541 SNIP 1.689 CiteScore 2.72
- Web of Science (2015): Indexed yes
- BFI (2014): BFI-level 2
- Scopus rating (2014): SJR 0.582 SNIP 1.901 CiteScore 2.48
- Web of Science (2014): Indexed yes
- BFI (2013): BFI-level 2
- Scopus rating (2013): SJR 0.642 SNIP 2.498 CiteScore 3.11
- ISI indexed (2013): ISI indexed yes
- BFI (2012): BFI-level 2
- Scopus rating (2012): SJR 0.655 SNIP 2.184 CiteScore 2.85
- ISI indexed (2012): ISI indexed yes
- Web of Science (2012): Indexed yes
- BFI (2011): BFI-level 2
- Scopus rating (2011): SJR 0.716 SNIP 2.281 CiteScore 3.13
- ISI indexed (2011): ISI indexed yes
- BFI (2010): BFI-level 2
- Scopus rating (2010): SJR 0.663 SNIP 2.024
- BFI (2009): BFI-level 2
- Scopus rating (2009): SJR 0.738 SNIP 1.861
- Web of Science (2009): Indexed yes
- BFI (2008): BFI-level 2
- Scopus rating (2008): SJR 0.775 SNIP 1.848
- Web of Science (2008): Indexed yes
- Scopus rating (2007): SJR 0.819 SNIP 1.867
- Scopus rating (2006): SJR 0.754 SNIP 1.661
- Scopus rating (2005): SJR 0.801 SNIP 1.917
- Scopus rating (2004): SJR 0.824 SNIP 1.907
- Scopus rating (2003): SJR 0.706 SNIP 1.838
- Scopus rating (2002): SJR 0.593 SNIP 1.363
- Scopus rating (2001): SJR 0.527 SNIP 0.992
- Scopus rating (2000): SJR 0.343 SNIP 0.851
Redundancy Optimization for Error Recovery in Digital Microfluidic Biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate all the necessary functions for biochemical analysis. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets. Researchers have proposed approaches for the synthesis of digital microfluidic biochips, which, starting from a biochemical application and a given biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. During the execution of a bioassay, operations could experience transient errors (e.g., erroneous droplet volumes), thus impacting negatively the correctness of the application. Researchers have proposed fault-tolerance approaches, which apply predetermined recovery actions at the moment when errors are detected. In this paper, we propose an online recovery strategy, which decides during the execution of the biochemical application the introduction of the redundancy required for fault-tolerance. We consider both time redundancy, i.e., re-executing erroneous operations, and space redundancy, i.e., creating redundant droplets for fault-tolerance. Error recovery is performed such that the number of transient errors tolerated is maximized and the timing constraints of the biochemical application are satisfied. The proposed redundancy optimization approach has been evaluated using several benchmarks.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alistar, M. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Pages: 129-159
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication information

Journal: Design Automation for Embedded Systems
Volume: 19
Issue number: 1-2
ISSN (Print): 0929-5585
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 0.428 SJR 0.172
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
Scopus rating (2016): SJR 0.171 SNIP 0.513 CiteScore 0.62
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.165 SNIP 0.449 CiteScore 0.71
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.155 SNIP 0.23 CiteScore 0.62
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 0.2 SNIP 0.757 CiteScore 0.67
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.166 SNIP 0.642 CiteScore 0.59
ISI indexed (2012): ISI indexed yes
Web of Science (2012): Indexed yes
Reliability in Warehouse-Scale Computing: Why Low Latency Matters

Warehouse sized buildings are nowadays hosting several types of large computing systems: from supercomputers to large clusters of servers to provide the infrastructure to the cloud. Although the main target, especially for high-performance computing, is still to achieve high throughput, the limiting factor of these warehouse-scale data centers is the power dissipation. Power is dissipated not only in the computation itself, but also in heat removal (fans, air conditioning, etc.) to keep the temperature of the devices within the operating ranges. The need to keep the temperature low within a minimal power envelope and to maintain high throughput and high reliability poses hard challenges.

In this work, we show that by moving part of the computation to accelerators, not only we reduce the latency of operations, but also make the system more energy efficient and reliable.
Safety-critical Java on a time-predictable processor

For real-time systems the whole execution stack needs to be time-predictable and analyzable for the worst-case execution time (WCET). This paper presents a time-predictable platform for safety-critical Java. The platform consists of (1) the Patmos processor, which is a time-predictable processor; (2) a C compiler for Patmos with support for WCET analysis; (3) the HVM, which is a Java-to-C compiler; (4) the HVM-SCJ implementation which supports SCJ Level 0, 1, and 2 (for both single and multicore platforms); and (5) a WCET analysis tool.

We show that real-time Java programs translated to C and compiled to a Patmos binary can be analyzed by the AbsInt aiT WCET analysis tool. To the best of our knowledge the presented system is the second WCET analyzable real-time Java system; and the first one on top of a RISC processor.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, VIA University College
Authors: Korsholm, S. E. (Ekstern), Schoeberl, M. (Intern), Puffitsch, W. (Intern)
Number of pages: 9
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 13th International Workshop on Java Technologies for Real-time and Embedded Systems (JTRES ’15)
Publisher: Association for Computing Machinery
Article number: 3
ISBN (Print): 978-1-4503-3644-4
BFI conference series: International workshop on Java technologies for real-time and embedded systems (5000304)
Main Research Area: Technical/natural sciences
Safety-Critical Java, Hardware locks, Synchronization
DOIs:
10.1145/2822304.2822309
Source: PublicationPreSubmission
Source-ID: 118024732
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Scala for Real-Time Systems?

Java served well as a general-purpose language. However, during its two decades of constant change it has gotten some weight and legacy in the language syntax and the libraries. Furthermore, Java's success for real-time systems is mediocre.

Scala is a modern object-oriented and functional language with interesting new features. Although a new language, it executes on a Java virtual machine, reusing that technology. This paper explores Scala as language for future real-time systems.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schoeberl, M. (Intern)
Number of pages: 5
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 13th International Workshop on Java Technologies for Real-time and Embedded Systems (JTRES ‘15)
Publisher: Association for Computing Machinery
Article number: 13
ISBN (Print): 978-1-4503-3644-4
BFI conference series: International workshop on Java technologies for real-time and embedded systems (5000304)
Main Research Area: Technical/natural sciences
Real-time systems, Scala, Real-time Java
DOIs:
Stack Caching Using Split Data Caches
In most embedded and general purpose architectures, stack data and non-stack data is cached together, meaning that writing to or loading from the stack may expel non-stack data from the data cache. Manipulation of the stack has a different memory access pattern than that of non-stack data, showing higher temporal and spatial locality. We propose caching stack and non-stack data separately and develop four different stack caches that allow this separation without requiring compiler support. These are the simple, window, and prefilling with and without tag stack caches. The performance of the stack cache architectures was evaluated using the SimpleScalar toolset where the window and prefilling stack cache without tag resulted in an execution speedup of up to 3.5% for the MiBench benchmarks, executed on an out-of-order processor with the ARM instruction set.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Nielsen, C. (Ekstern), Schoeberl, M. (Intern)
Pages: 66-73
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 18th International Symposium on Real-Time Distributed Computing Workshops (ISORCW 2015)
Publisher: IEEE
ISBN (Print): 978-1-4799-7709-6
BFI conference series: Object-Oriented Real-Time Distributed Computing (5000415)
Main Research Area: Technical/natural sciences
Cache Memory, Microprocessors, Stack Caching
DOIs: 10.1109/ISORCW.2015.59
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Synthesis of Biochemical Applications on Digital Microfluidic Biochips with Operation Execution Time Variability
Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate all the necessary functions for biochemical analysis. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets. Several approaches have been proposed for the synthesis of digital microfluidic biochips, which, starting from a biochemical application and a given biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. Researchers have assumed that each biochemical operation in an application is characterized by a worst-case execution time (wcet). However, during the execution of the application, due to variability and randomness in biochemical reactions, operations may finish earlier than their wcets, resulting in unexploited slack in the schedule. In this paper, we first propose an online synthesis strategy that re-synthesizes the application at runtime when operations experience variability in their execution time, exploiting thus the slack to obtain shorter application completion times. We also propose a quasi-static synthesis strategy that determines offline a database of alternative implementations. During the execution of the application, several implementations are selected based on the current execution scenario with operation execution time variability. The proposed strategies have been evaluated using several benchmarks and compared to related work.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alistar, M. (Intern), Pop, P. (Intern)
Pages: 158-168
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication information
Journal: Integration
Volume: 51
Issue number: September
System-level synthesis of multi-ASIP platforms using an uncertainty model

In this paper we propose a system-level synthesis for MPSoCs that integrates multiple Application Specific Instruction Set Processors (ASIPs). Each ASIP is customized for a specific set of tasks. The system-level synthesis is responsible for assigning the tasks to the ASIPs, exploring different platform alternatives. We can allocate tasks to the different ASIPs and determine if the applications are schedulable only knowing the worst-case execution time (WCET) of each task. We can estimate the WCET only after establishing the micro-architecture of the ASIP. At the same time, an ASIP micro-architecture can be derived only knowing the assignment of tasks to ASIP. To address this circular dependency, we propose an Uncertainty Model for the WCETs, which captures the performance of tasks running on a range of possible ASIP implementations. We propose a novel stochastic schedulability analysis to evaluate each multi-ASIP platform. We
use an Evolutionary Algorithm-based approach to explore the design space of macro-architecture possibilities and we evaluate it using real case studies.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Micconi, L. (Intern), Madsen, J. (Intern), Pop, P. (Intern)
Pages: 118-138
Publication date: 2015
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Integration
Volume: 51
ISSN (Print): 0167-9260
Ratings:
- BFI (2018): BFI-level 1
- Web of Science (2018): Indexed yes
- BFI (2017): BFI-level 1
- Scopus rating (2017): SNIP 0.869 SJR 0.223
- Web of Science (2017): Indexed Yes
- BFI (2016): BFI-level 1
- Scopus rating (2016): SJR 0.215 SNIP 1.035 CiteScore 1.25
- BFI (2015): BFI-level 1
- Scopus rating (2015): SJR 0.246 SNIP 1.123 CiteScore 1.09
- Web of Science (2015): Indexed yes
- BFI (2014): BFI-level 1
- Scopus rating (2014): SJR 0.295 SNIP 1.168 CiteScore 1.19
- BFI (2013): BFI-level 1
- Scopus rating (2013): SJR 0.306 SNIP 0.986 CiteScore 1.28
- ISI indexed (2013): ISI indexed yes
- BFI (2012): BFI-level 1
- Scopus rating (2012): SJR 0.228 SNIP 1.183 CiteScore 1.19
- ISI indexed (2012): ISI indexed yes
- BFI (2011): BFI-level 1
- Scopus rating (2011): SJR 0.299 SNIP 0.826 CiteScore 1.23
- ISI indexed (2011): ISI indexed yes
- BFI (2010): BFI-level 1
- Scopus rating (2010): SJR 0.255 SNIP 0.895
- BFI (2009): BFI-level 1
- Scopus rating (2009): SJR 0.289 SNIP 0.927
- BFI (2008): BFI-level 1
- Scopus rating (2008): SJR 0.256 SNIP 0.809
- Scopus rating (2007): SJR 0.525 SNIP 1.59
- Scopus rating (2006): SJR 0.305 SNIP 0.936
- Scopus rating (2005): SJR 0.244 SNIP 0.994
- Scopus rating (2004): SJR 0.175 SNIP 0.608
- Scopus rating (2003): SJR 0.398 SNIP 0.688
- Scopus rating (2002): SJR 0.163 SNIP 0.543
- Scopus rating (2001): SJR 0.167 SNIP 0.129
- Scopus rating (2000): SJR 0.16 SNIP 0.226
- Scopus rating (1999): SJR 0.167 SNIP 0.681

Original language: English

**System-level design, Multi-ASIP, Probabilistic model, Early design**

**DOIs:**
- 10.1016/j.vlsi.2015.07.006

Source: FindIt
**T-CREST: Time-predictable multi-core architecture for embedded systems**

Real-time systems need time-predictable platforms to allow static analysis of the worst-case execution time (WCET). Standard multi-core processors are optimized for the average case and are hardly analyzable. Within the T-CREST project we propose novel solutions for time-predictable multi-core architectures that are optimized for the WCET instead of the average-case execution time. The resulting time-predictable resources (processors, interconnect, memory arbiter, and memory controller) and tools (compiler, WCET analysis) are designed to ease WCET analysis and to optimize WCET performance. Compared to other processors the WCET performance is outstanding. The T-CREST platform is evaluated with two industrial use cases. An application from the avionic domain demonstrates that tasks executing on different cores do not interfere with respect to their WCET. A signal processing application from the railway domain shows that the WCET can be reduced for computation-intensive tasks when distributing the tasks on several cores and using the network-on-chip for communication. With three cores the WCET is improved by a factor of 1.8 and with 15 cores by a factor of 5.7. The T-CREST project is the result of a collaborative research and development project executed by eight partners from academia and industry. The European Commission funded T-CREST.

**General information**

State: Published
Pages: 449-471
Publication date: 2015
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Journal of Systems Architecture
Volume: 61
Issue number: 9
ISSN (Print): 1383-7621
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 1.121 SJR 0.255
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 2
Scopus rating (2016): SJR 0.32 SNIP 1.208 CiteScore 1.66
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.306 SNIP 0.995 CiteScore 1.39
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 2
Scopus rating (2014): SJR 0.296 SNIP 1.195 CiteScore 1.14
BFI (2013): BFI-level 2
Scopus rating (2013): SJR 0.29 SNIP 1.318 CiteScore 1.32
ISI indexed (2013): ISI indexed yes
BFI (2012): BFI-level 2
Scopus rating (2012): SJR 0.314 SNIP 1.153 CiteScore 1.51
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 2
Scopus rating (2011): SJR 0.272 SNIP 1.109 CiteScore 1.23
ISI indexed (2011): ISI indexed yes
BFI (2010): BFI-level 2
Scopus rating (2010): SJR 0.351 SNIP 1.07
Test-driven modeling of embedded systems

To benefit maximally from model-based systems engineering (MBSE) trustworthy high quality models are required. From the software disciplines it is known that test-driven development (TDD) can significantly increase the quality of the products. Using a test-driven approach with MBSE may have a similar positive effect on the quality of the system models and the resulting products and may therefore be desirable. To define a test-driven model-based systems engineering (TDD-MBSE) approach, we must define this approach for numerous sub disciplines such as modeling of requirements, use cases, scenarios, behavior, architecture, etc. In this paper we present a method that utilizes the formalism of timed automata with formal and statistical model checking techniques to apply TDD-MBSE to the modeling of system architecture and behavior. The results obtained from applying it to an industrial case suggest that our method provides a sound foundation for rapid development of high quality system models.

The Argo NOC: Combining TDM and GALS

Argo is a network-on-chip developed for use in a multi-core platform designed specifically for hard real-time applications and it supports message passing across virtual end-to-end channels. Argo implements these channels using time-division-multiplexing (TDM) of the resources in the NOC following a static schedule. This requires some form of global synchrony
across the platform. At the same time it is generally accepted that a large chip should employ some form of globally-asynchronous locally-synchronous (GALS) organization. By using asynchronous routers and by rethinking the microarchitecture of the network interfaces we have managed to combine TDM and GALS and obtain a very hardware-efficient implementation of the NOC. The paper gives a brief overview of the Argo NOC and focuses on two important issues: how to safely bring the NOC out of reset and timing analysis of the network of asynchronous routers.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Applied Mathematics and Computer Science
Authors: Kasapaki, E. (Intern), Sparse, J. (Intern)
Number of pages: 4
Publication date: 2015

Host publication information
Title of host publication: Proceedings of the 22nd European Conference on Circuit Theory and Design (ECCTD 2015)
Publisher: IEEE
ISBN (Print): 978-1-4799-9877-7
BFI conference series: European Conference on Circuit Theory and Design (5010330)
Main Research Area: Technical/natural sciences
Conference: 22nd European conference on circuit theory and design, Trondheim, Norway, 24/08/2015 - 24/08/2015
DOIs: 10.1109/ECCTD.2015.7300101
Source: FindIt
Source-ID: 276537292
Publication: Research - peer-review › Article in proceedings – Annual report year: 2015

Thermal Aware Floorplanning Incorporating Temperature Dependent Wire Delay Estimation
Temperature has a negative impact on metal resistance and thus wire delay. In state-of-the-art VLSI circuits, large thermal gradients usually exist due to the uneven distribution of heat sources. The difference in wire temperature can lead to performance mismatch because wires of the same length can have different delay.

Traditional floorplanning algorithms use wirelength to estimate wire performance. In this work, we show that this does not always produce a design with the shortest delay and we propose a floorplanning algorithm taking into account temperature dependent wire delay as one metric in the evaluation of a floorplan. In addition, we consider other temperature dependent factors such as congestion and interconnect reliability.

The experiment results show that a shorter delay can be achieved using the proposed method.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Knowles Electronics, Oticon A/S, Arizona State University
Authors: Winther, A. (Ekstern), Liu, W. (Ekstern), Nannarelli, A. (Intern), Vrudhula, S. (Ekstern)
Pages: 807-815
Publication date: 2015
Main Research Area: Technical/natural sciences

Publication information
Journal: Microprocessors and Microsystems
Volume: 39
Issue number: 8
ISSN (Print): 0141-9331
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 0.771 SJR 0.24
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 1.11 SJR 0.225 SNIP 0.822
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.25 SNIP 0.857 CiteScore 0.89
Time-division multiplexing vs network calculus: A comparison

Networks-on-chip are increasingly common in modern multicore architectures. However, general-purpose networks-on-chip are not always well suited for real-time applications that require bandwidth and latency guarantees. Two approaches to provide real-time guarantees have emerged: time-division multiplexing, where traffic is scheduled according to a precalculated static schedule, and network calculus, a mathematical framework to reason about dynamically scheduled networks. This paper compares the two approaches to provide insight into their relative advantages and disadvantages. The results show that time-division multiplexing leads to better worst-case latencies, while network calculus supports higher bandwidths. Furthermore, time-division multiplexing leads to a simpler hardware implementation, while dynamically scheduled networks-on-chip allow the integration of best-effort traffic in the on-chip network in a more natural way.
Timing Analysis of Rate Constrained Traffic for the TTEthernet Communication Protocol

Ethernet is a low-cost communication solution offering high transmission speeds. Although its applications extend beyond computer networking, Ethernet is not suitable for real-time and safety-critical systems. To alleviate this, several real-time Ethernet-based communication protocols have been proposed, such as TTEthernet, which is the focus of this paper.

TTEthernet is suitable for mixed-criticality systems both in the safety and temporal domain. TTEthernet offers three traffic classes: static time-triggered (TT) traffic, dynamic traffic with bounded transmission rate (called "Rate Constrained", RC), and unbounded dynamic traffic ("Best-Effort", BE). In this paper we propose a novel worst-case end-to-end delay analysis of the RC traffic for TTEthernet systems. The proposed technique considerably reduces the pessimism of the analysis, compared to existing approaches. We have evaluated the new analysis using several test cases.

Towards droplet size-aware biochemical application compilation for AM-EWOD biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate onchip all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets on an array of electrodes. Microfluidic operations, such as transport, mixing, split, are performed on this array by routing the corresponding droplets on a series of electrodes. Several approaches have been proposed for the compilation of digital microfluidic biochips, which, starting from a biochemical application and a given biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. To simplify the compilation problem, researchers have assumed an abstract droplet size of one electrode. However, the droplet size abstraction is not realistic and it impacts negatively the execution of the biochemical application, leading in most cases to its failure. Hence the existing compilation approaches have to be revisited to consider the size of the droplets. In this paper we take the first step towards a droplet size-aware compilation by proposing a routing algorithm that considers the droplet size. Our routing algorithm is developed for a novel digital microfluidic biochip architecture based on Active Matrix Electrowetting on Dielectric, which uses a thin film transistor array for the electrodes. We also implement a simulator that allows us to perform the needed adaptations and to validate the proposed routing algorithm.
Video Surveillance: Privacy Issues and Legal Compliance

Pervasive usage of video surveillance is rapidly increasing in developed countries. Continuous security threats to public safety demand use of such systems. Contemporary video surveillance systems offer advanced functionalities which threaten the privacy of those recorded in the video. There is a need to balance the usage of video surveillance against its negative impact on privacy. This chapter aims to highlight the privacy issues in video surveillance and provides a model to help identify the privacy requirements in a video surveillance system. The authors make a step in the direction of investigating the existing legal infrastructure for ensuring privacy in video surveillance and suggest guidelines in order to help those who want to deploy video surveillance while least compromising the privacy of people and complying with legal infrastructure.

vZ - An Optimizing SMT Solver

vZ is a part of the SMT solver Z3. It allows users to pose and solve optimization problems modulo theories. Many SMT applications use models to provide satisfying assignments, and a growing number of these build on top of Z3 to get optimal assignments with respect to objective functions. vZ provides a portfolio of approaches for solving linear optimization problems over SMT formulas, MaxSMT, and their combinations. Objective functions are combined as either Pareto fronts, lexicographically, or each objective is optimized independently. We describe usage scenarios of vZ, outline the tool architecture that allows dispatching problems to special purpose solvers, and examine use cases.
vZ - Maximal Satisfaction with Z3

Satisfiability Modulo Theories, SMT, solvers are used in many applications. These applications benefit from the power of tuned and scalable theorem proving technologies for supported logics and specialized theory solvers. SMT solvers are primarily used to determine whether formulas are satisfiable. Furthermore, when formulas are satisfiable, many applications need models that assign values to free variables. Yet, in many cases arbitrary assignments are insufficient, and what is really needed is an optimal assignment with respect to objective functions. So far, users of Z3, an SMT solver from Microsoft Research, build custom loops to achieve objective values. This is no longer necessary with νZ (new-Z, or max-Z), an extension within Z3 that lets users formulate objective functions directly with Z3. Under the hood there is a portfolio of approaches for solving linear optimization problems over SMT formulas, MaxSMT, and their combinations. Objective functions are combined as either Pareto fronts, lexicographically, or each objective is optimized independently.

Addressing production stops in the food industry

This paper investigates the challenges in the food industry which causes the production lines to stop, illustrated by a case study of an SME size company in the baked goods sector in Denmark. The paper proposes key elements this sector needs to be aware of to effectively address production stops, and gives examples of the unique challenges faced by the SME food industry.
A flexible mobile-device biosensing instrumentation platform for point-of-care medical diagnostics applications

General information
State: Published
Organisations: Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Department of Electrical Engineering, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Number of pages: 1
Publication date: 2014
Event: Poster session presented at 24th Anniversary World Congress on Biosensors, Melbourne, Australia.
Main Research Area: Technical/natural sciences
Source: PublicationPreSubmission
Source-ID: 101856297
Publication: Research - peer-review › Poster – Annual report year: 2014

The early diagnosis and monitoring of chronic diseases still constitutes today one of the major healthcare challenges in our society. Advances in nanotechnology and microfluidics have been increasingly empowering researchers and engineers with tools to develop integrated biosensing solutions helping to address this challenge. Specifically, Lab-on-Chip (LoC) devices have a key role to play in the advent of Point-of-Care (PoC) medical applications, driving a shift of the medical diagnostics paradigm and the transition from a centralized, technical, high-throughput biological sample analysis process to a doctor-patient and patient-oriented field decision-making support system.

The success of such systems requires the development of highly sensitive and specific biosensors to reliably detect small amounts of relevant biological markers. Nevertheless, the socio-technical complexity of the PoC medical diagnostics context necessitates considering broader requirements, notably in terms of usability, flexibility, and integration capabilities. These characteristics call for multi-disciplinary design methodologies inspired from the field of systems engineering and constitute the motivations for this work.

We present a mobile-device based, PoC biosensing instrumentation platform, designed for multiplexed high-impedance sensing and the electrochemical detection of biological species on a LoC. The proposed system is thus designed as a flexible, user-friendly hardware and software platform allowing programmable electrical readout from LoCs potentially comprehending various transducers targeting different biological markers. A smartphone/tablet docking-station embeds the hardware interface necessary for the implementation of a smartphone digital lock-in amplifier. The platform is tested with high-impedimetric measurements from silicon-nanowire field effect transistors embedded in a LoC. Programmable firmware and flexible hardware will in turn allow for standard voltammetry and electrical impedance spectroscopy to be performed. The design of a mobile app and standard mobile software libraries will ensure system evolvability, enabling application-specific biosensors readouts and adapted user interfacing.
Alignment of Memory Transfers of a Time-Predictable Stack Cache

Modern computer architectures use features which often complicate the WCET analysis of real-time software. Alternative time-predictable designs, and in particular caches, thus are gaining more and more interest. A recently proposed stack cache, for instance, avoids the need for the analysis of complex cache states. Instead, only the occupancy level of the cache has to be determined.

The memory transfers generated by the standard stack cache are not generally aligned. These unaligned accesses risk to introduce complexity to the otherwise simple WCET analysis. In this work, we investigate three different approaches to handle the alignment problem in the stack cache: (1) unaligned transfers, (2) alignment through compiler-generated padding, (3) a novel hardware extension ensuring the alignment of all transfers. Simulation results show that our hardware extension offers a good compromise between average-case performance and analysis complexity.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, ENSTA ParisTech
Authors: Abbaspourseyyedi, S. (Intern), Brandner, F. (Ekstern)
Pages: 17-20
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 8th Junior Researcher Workshop on Real-Time Computing (JRWRTC 2014)
Main Research Area: Technical/natural sciences
Workshop: 8th Junior Researcher Workshop on Real-Time Computing (JRWRTC 2014), Versailles, France, 08/10/2014
Block-Aligned Stack Cache, Alignment, Real-Time Systems
Electronic versions:
scba.pdf
Links:
Source: PublicationPreSubmission
Source-ID: 100853014
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A Loosely Synchronizing Asynchronous Router for TDM-Scheduled NOCs
This paper presents an asynchronous router design for use in time-division-multiplexed (TDM) networks-on-chip. Unlike existing synchronous, mesochronous and asynchronous router designs with similar functionality, the router is able to silently skip over cycles/TDM-slots where no traffic is scheduled and hence avoid all switching activity in the idle links and router ports. In this way switching activity is reduced to the minimum possible amount.

The fact that this relaxed synchronization is sufficient to implement TDM scheduling represents a contribution at the conceptual level. The idea can only be implemented using asynchronous circuit techniques. To this end, the paper explores the use of “click-element” templates. Click-element templates use only flipflops and conventional gates, and this greatly simplifies the design process when using conventional EDA tools and standard cell libraries. Few papers, if any, have explored this.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark, ENSTA ParisTech
Authors: Kotleas, I. (Ekstern), Humphreys, D. (Ekstern), Sørensen, R. B. (Intern), Kasapaki, E. (Intern), Brandner, F. (Ekstern), Sparsø, J. (Intern)
Pages: 151-158
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 8th IEEE/ACM International Symposium on Networks-on-Chip (NOCS) 2014
Publisher: IEEE
Editors: Bertozzi, D., Benini, L., Yalamanchili, S., Henkel, J.
ISBN (Print): 978-1-4799-5347-9
BFI conference series: Networks-on-Chips (500385)
Main Research Area: Technical/natural sciences
DOIs:
10.1109/NOCS.2014.7008774
Source: PublicationPreSubmission

In receiver-initiated medium access control (MAC) protocols for wireless sensor networks, communication is initiated by the receiver node which transmits beacons indicating its availability to receive data. In the case of multiple senders having traffic for a given receiver, such beacons form points where collisions are likely to happen. In this paper, we present altruistic backoff (AB), a novel collision avoidance mechanism that aims to avoid collisions before the transmission of a beacon. As a result of an early backoff, senders spend less time in idle listening waiting for a beacon, thus saving significant amounts of energy. We present an implementation of AB for Texas Instruments’ eZ430-rf2500 sensor nodes and we evaluate its performance with simulations and experiments.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Fafoutis, X. (Intern), Orfanidis, C. (Ekstern), Dragoni, N. (Intern)
Number of pages: 11
Publication date: 2014
Main Research Area: Technical/natural sciences

Publication information
Journal: International Journal of Distributed Sensor Networks
Volume: 2014
Article number: 576401
ISSN (Print): 1550-1329
Ratings:
Web of Science (2018): Indexed yes
Scopus rating (2017): SNIP 0.745 SJR 0.255
Web of Science (2017): Indexed Yes
Scopus rating (2016): CiteScore 1.16 SJR 0.256 SNIP 0.727
Scopus rating (2015): SJR 0.256 SNIP 0.877 CiteScore 1.1
Web of Science (2015): Indexed yes
Scopus rating (2014): SJR 0.242 SNIP 0.699 CiteScore 0.85
Web of Science (2014): Indexed yes
Scopus rating (2013): SJR 0.231 SNIP 0.899 CiteScore 1.13
Scopus rating (2012): SJR 0.192 SNIP 0.586 CiteScore 0.87
Scopus rating (2011): SJR 0.16 SNIP 0.44 CiteScore 0.53
Scopus rating (2010): SJR 0.146 SNIP 0.237
Scopus rating (2009): SJR 0.303 SNIP 0.78
Web of Science (2009): Indexed yes
Scopus rating (2008): SJR 0.287 SNIP 0.919
Scopus rating (2007): SJR 0.193 SNIP 1.045
Original language: English
Electronic versions:
Hindawi576401.pdf
DOI: 10.1155/2014/576401

Bibliographical note
Article ID 576401
Source: FindIt
Source-ID: 270266855
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A Metaheuristic Scheduler for Time Division Multiplexed Network-on-Chip

This report presents a metaheuristic scheduler for inter-processor communication in multi-core platforms using time division multiplexed (TDM) networks on chip (NOC). Input to the scheduler is a specification of the target multi-core platform and a specification of the application. Compared to previous works, the scheduler handles a broader and more general class of platforms.
Another contribution, which has significant practical implications, is the minimization of the TDM schedule period by overprovisioning bandwidth to connections with the smallest bandwidth requirements. Our results show that this is possible with only negligible impact on the schedule period.

We evaluate the scheduler with seven different applications from the MCSL NOC benchmark suite. We observe that the metaheuristics perform better than the greedy solution. In the special case of all-to-all communication with equal bandwidths on all communication channels, we obtain schedules with a shorter period than reported in previous work.
A method cache for Patmos
For real-time systems we need time-predictable processors. This paper presents a method cache as a time-predictable solution for instruction caching. The method cache caches whole methods (or functions) and simplifies worst-case execution time analysis. We have integrated the method cache in the time-predictable processor Patmos. We evaluate the method cache with a large set of embedded benchmarks. Most benchmarks show a good hit rate for a method cache size in the range between 4 and 16 KB.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering, Vienna University of Technology
Authors: Degasperi, P. (Ekstern), Hepp, S. (Ekstern), Puffitsch, W. (Intern), Schoeberl, M. (Intern)
Pages: 100-108
Publication date: 2014
BFI conference series: Object-Oriented Real-Time Distributed Computing (5000415)
Main Research Area: Technical/natural sciences

Publication information
Journal: International Symposium on Object-Oriented Real-Time Distributed Computing
ISSN (Print): 1555-0885
Ratings:
BFI (2018): BFI-level 1
BFI (2017): BFI-level 1
BFI (2016): BFI-level 1
BFI (2015): BFI-level 1
BFI (2014): BFI-level 1
BFI (2013): BFI-level 1
ISI indexed (2013): ISI indexed no
BFI (2012): BFI-level 1
ISI indexed (2012): ISI indexed no
ISI indexed (2011): ISI indexed no
Original language: English
Computing and Processing, caches, Computer architecture, Hardware, Object oriented modeling, Pipelines, real-time systems, Resource management, System-on-chip, time-predictable architecture
DOIs: 10.1109/ISORC.2014.47
Source: FindIt
Source-ID: 271793040
Publication: Research - peer-review › Conference article – Annual report year: 2014

An evaluation of safety-critical Java on a Java processor
The safety-critical Java (SCJ) specification provides a restricted set of the Java language intended for applications that require certification. In order to test the specification, implementations are emerging and the need to evaluate those implementations in a systematic way is becoming important. In this paper we evaluate our SCJ implementation which is based on the Java Optimized Processor JOP and we measure different performance and timeliness criteria relevant to hard real-time systems. Our implementation targets Level 0 and Level1 of the specification and to test it we use a series of micro benchmarks, an application-based benchmark, and a reduced set of a SCJ technology compatibility kit. We evaluate the accuracy of periods, linear-time memory allocation, aperiodic event handling, dispatch latency for interrupts, context switch preemption latency, and synchronization.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering
Authors: Rios Rivas, J. R. (Intern), Schoeberl, M. (Intern)
Pages: 276-283
Publication date: 2014

Host publication information
Title of host publication: 2014 IEEE 17th International Symposium on Object/Component/Service-Oriented Real-Time Distributed Computing (ISORC)
Publisher: IEEE
A novel single-step, multipoint calibration method for instrumented Lab-on-Chip systems

Despite recent and substantial advances in biosensing, information and communication, and Lab-on-Chip (LoC) technologies, the success of Point-of-Care (PoC) diagnostics and monitoring systems is still challenged by stringent requirements for robustness, cost-effectiveness, and system integration.

The pitfalls of PoC system adoption can be addressed early in the system design phase. They require a multidisciplinary design approach supported by systems engineering tools and methods. Considering this, we here present both a model and an implementation of a simple and rapid calibration scheme for instrument-based PoC blood biomarker analysis systems. Motivated by the complexity of associating high-accuracy biosensing using silicon nanowire field effect transistors with ease of use for the PoC system user, we propose a novel one-step, multipoint calibration method for LoC-based systems. Our approach specifically addresses the important interfaces between a novel microfluidic unit to integrate the sensor array and a mobile-device hardware accessory. A multi-point calibration curve is obtained by generating a defined set of reference concentrations from a single input. By consecutively splitting the flow perpendicular to the diffusion interface only one mixing step is required for each of the generated calibration solutions. This results in a compact design with a very small footprint of the microfluidic layout.

General information
State: Published
Organisations: Department of Micro- and Nanotechnology, Nano Bio Integrated Systems, Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Number of pages: 1
Publication date: 2014
Event: Poster session presented at Lab-on-a-Chip European Congress 2014, Berlin, Germany.
Main Research Area: Technical/natural sciences
Electronic versions: Poster_LoC_2014VER1.pdf
Source: PublicationPreSubmission
Source-ID: 101678079
Publication: Research - peer-review › Poster – Annual report year: 2014
A practical approach to model checking Duration Calculus using Presburger Arithmetic

This paper investigates the feasibility of reducing a model-checking problem K ⊧ ϕ for discrete time Duration Calculus to the decision problem for Presburger Arithmetic. Theoretical results point at severe limitations of this approach: (1) the reduction in Fränzle and Hansen (Int J Softw Inform 3(2–3):171–196, 2009) produces Presburger formulas whose sizes grow exponentially in the chop-depth of ϕ, where chop is an interval modality originating from Moszkowski (IEEE Comput 18(2):10–19, 1985), and (2) the decision problem for Presburger Arithmetic has a double exponential lower bound and a triple exponential upper bound. The generated Presburger formulas have a rich Boolean structure, many quantifiers and quantifier alternations. Such formulas are simplified using so-called guarded formulas, where a guard provides a context used to simplify the rest of the formula. A normal form for guarded formulas supports global effects of local simplifications. Combined with quantifier-elimination techniques, this normalization gives significant reductions in formula sizes and in the number of quantifiers. As an example, we solve a configuration problem using the SMT-solver Z3 as backend. Benefits and the current limits of the approach are illustrated by a family of examples.
Argo: A Time-Elastic Time-Division-Multiplexed NOC using Asynchronous Routers

In this paper we explore the use of asynchronous routers in a time-division-multiplexed (TDM) network-on-chip (NOC), Argo, that is being developed for a multi-processor platform for hard real-time systems. TDM inherently requires a common time reference, and existing TDM-based NOC designs are either synchronous or mesochronous. We use asynchronous routers to achieve a simpler, smaller, and more robust, self-timed design. Our design exploits the fact that pipelined asynchronous circuits also behave as ripple FIFOs. Thus, it avoids the need for explicit synchronization FIFOs between the routers. Argo has interesting elastic timing properties that allow it to tolerate skew between the network interfaces (NIs).

The paper presents Argo NOC-architecture and provides a quantitative analysis of its ability of absorb skew between the NIs. Using a signal transition graph model and realistic component delays derived from a 65nm CMOS implementation, a worstcase analysis shows that a typical design can tolerate a skew of 1-5 cycles (depending on FIFO depths and NI clock frequency). Simulation results of a 2 x 2 NOC confirm this.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Kasapaki, E. (Intern), Sparsø, J. (Intern)
Pages: 45-52
Publication date: 2014

Host publication information
Publisher: IEEE

Series: International Symposium on Advanced Research in Asynchronous Circuits and Systems
ISSN: 1522-8681
BFI conference series: Symposium on Asynchronous Circuits and Systems (5000027)
Main Research Area: Technical/natural sciences
Conference: 20th IEEE International Symposium on Asynchronous Circuits and Systems (ASYNC) 2014, Postdam, Germany, 12/05/2014 - 12/05/2014
DOIs: 10.1109/ASYNC.2014.14
Source: PublicationPreSubmission
Source-ID: 101067483
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014
A Synthesizable Multicore Platform for Microwave Imaging

Active microwave imaging techniques such as radar and tomography are used in a wide range of medical, industrial, scientific, and military applications. Microwave imaging devices emit radio waves and process their reflections to reconstruct an image. However, data processing remains a challenge as image reconstruction algorithms are computationally expensive and many applications come with strictly constrained mechanical or power requirements. We developed Tinuso, a multicore architecture optimized for performance when implemented on an FPGA. Tinuso’s architecture is well suited to run highly parallel image reconstruction applications at a low power budget. In this paper, we describe the design and the implementation of Tinuso’s communication structures, which include a generic 2D mesh on-chip interconnect and a network interface to the processor pipeline. We optimize the network for a latency of one cycle per network hop and attain a high clock frequency by pipelining the feedback loop to manage contention. We implement a multicore configuration with 48 cores and achieve a clock frequency as high as 300 MHz with a peak switching data rate of 9.6 Gbits/s per link on state-of-the-art FPGAs.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schleuniger, P. (Intern), Karlsson, S. (Intern)
Pages: 197-204
Publication date: 2014

Host publication information
Title of host publication: Reconfigurable Computing: Architectures, Tools, and Applications. Proceedings
Publisher: Springer
ISBN (Print): 978-3-319-05959-4
ISBN (Electronic): 978-3-319-05960-0

Series: Lecture Notes in Computer Science
Volume: 8405
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
Conference: 10th International Symposium on Reconfigurable Computing, Algarve, Portugal, 14/04/2014 - 14/04/2014
DOIs:
10.1007/978-3-319-05960-0_18
Source: FindIt
Source-ID: 266830920
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A Time-predictable Memory Network-on-Chip

To derive safe bounds on worst-case execution times (WCETs), all components of a computer system need to be time-predictable: the processor pipeline, the caches, the memory controller, and memory arbitration on a multicore processor. This paper presents a solution for time-predictable memory arbitration and access for chip-multiprocessors. The memory network-on-chip is organized as a tree with time-division multiplexing (TDM) of accesses to the shared memory. The TDM based arbitration completely decouples processor cores and allows WCET analysis of the memory accesses on individual cores without considering the tasks on the other cores. Furthermore, we perform local, distributed arbitration according to the global TDM schedule. This solution avoids a central arbiter and scales to a large number of processors.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Schoeberl, M. (Intern), Chong, D. V. (Ekstern), Puffitsch, W. (Intern), Sparse, J. (Intern)
Pages: 53-62
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 14th International Workshop on Worst-Case Execution Time Analysis (WCET 2014)
Publisher: OASICS
Editor: Falk, H.
ISBN (Electronic): 978-3-939897-69-9

Series: Open Access Series in Informatics
Volume: 39
ISSN: 2190-6807
Automated evolutionary restructuring of workflows to minimise errors via stochastic model checking
This paper presents a framework for the automated restructuring of workflows that allows one to minimise the impact of errors on a production workflow. The framework allows for the modelling of workflows by means of a formalised subset of the Business Process Modelling and Notation (BPMN) language, a well-established visual language for modelling workflows in a business context. The framework’s modelling language is extended to include the tracking of real-valued quantities associated with the process (such as time, cost, temperature). In addition, this language also allows for an intention preserving stochastic semantics able to model both probabilistic- or non-deterministic branching behaviour. We further extend this formalism to allow for the introduction of error states which allow for both fail-stop behaviour and continued system execution. We explore the practical utility of this approach by means of a case study from the food industry. Through this case study we explore the extent to which the risk of production faults can be reduced and the impact of these can be minimised, primarily through restructuring of the production workflows. This approach is fully automated and only the modelling of the production workflows and the expression of the goals require manual input.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Applied Mathematics and Computer Science , Department of Management Engineering, Management Science
Authors: Herbert, L. T. (Intern), Hansen, Z. N. L. (Intern), Jacobsen, P. (Intern)
Number of pages: 12
Publication date: 2014

Host publication information
Title of host publication: Proceedings of Probabilistic Safety Assessment and Management conference (PSAM12)
Main Research Area: Technical/natural sciences
Conference: Probabilistic Safety Assessment and Management conference 2014, Honolulu, HI, United States, 22/06/2014 - 22/06/2014
Consequence Modeling and Management, Enterprise Risk Management, Industrial Safety and Accident Analysis, Reliability Analysis and Risk Assessment Methods, Safety Assessment Software Tools, Safety Management and Decision Making
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Automatic generation of application specific FPGA multicore accelerators
High performance computing systems make increasing use of hardware accelerators to improve performance and power properties. For large high-performance FPGAs to be successfully integrated in such computing systems, methods to raise the abstraction level of FPGA programming are required. In this paper we propose a tool flow, which automatically generates highly optimized hardware multicore systems based on parameters. Profiling feedback is used to adjust these parameters to improve performance and lower the power consumption. For an image processing application we show that our tools are able to identify optimal performance energy trade-offs points for a multicore based FPGA accelerator.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering, Language-Based Technology
Pages: 1440-1444
Publication date: 2014
Certifiable Java for Embedded Systems

The Certifiable Java for Embedded Systems (CJ4ES) project aimed to develop a prototype development environment and platform for safety-critical software for embedded applications. There are three core constituents: A profile of the Java programming language that is tailored for safety-critical applications, a predictable Java processor built with FPGA technology, and an Eclipse based application development environment that binds the profile and the platform together and provides analyses that help to provide evidence that can be used as part of a safety case. This paper summarizes key contributions within these areas during the three-year project period. In the conclusion the overall result of the project is assessed.

Code Commentary and Automatic Refactorings using Feedback from Multiple Compilers

Optimizing compilers are essential to the performance of parallel programs on multi-core systems. It is attractive to expose parallelism to the compiler letting it do the heavy lifting. Unfortunately, it is hard to write code that compilers are able to optimize aggressively and therefore tools exist that can guide programmers with refactorings allowing the compilers to optimize more aggressively. We target the problem with many false positives that these tools often generate, where the amount of feedback can be overwhelming for the programmer. Our approach is to use a filtering scheme based on feedback from multiple compilers and show how we are able to filter out 87.6% of the comments by only showing the most promising comments.
Compilation and Synthesis for Fault-Tolerant Digital Microfluidic Biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, by integrating all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips (DMBs) manipulate discrete amounts of fluids of nanoliter volume, named droplets, on an array of electrodes to perform operations such as dispensing, transport, mixing, split, dilution and detection.

Researchers have proposed compilation approaches, which, starting from a biochemical application and a biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. During the execution of a bioassay, operations could experience transient faults, thus impacting negatively the correctness of the application. We have proposed both offline (design time) and online (runtime) recovery strategies. The online recovery strategy decides the introduction of the redundancy required for fault-tolerance. We consider both time redundancy, i.e., re-executing erroneous operations, and space redundancy, i.e., creating redundant droplets for fault-tolerance. Error recovery is performed such that the number of transient faults tolerated is maximized and the timing constraints of the biochemical application are satisfied.

Previous work has assumed that the biochip architecture is given, and most approaches consider a rectangular shape for the electrode array, where operations execute on rectangular “modules” formed of electrodes. However, non-regular application-specific architectures are common in practice. Hence, we have proposed an approach to the synthesis of application-specific architectures, such that the cost is minimized and the timing constraints of the application are satisfied.

We propose an algorithm to build a library of non-regular modules for a given applicationspecific architecture, so that the area of a non-regular application-specific biochip can be used effectively. During fabrication, DMBs can be affected by permanent faults, which may lead to the failure of the application. Our approach introduces redundant electrodes to synthesize fault-tolerant architectures aiming at increasing the yield of DMBs. We also propose a method to estimate, at design time, the application completion time in case of permanent faults in order to verify if an application can be successfully run on the architecture.

The proposed approaches were evaluated using several real-life case studies and synthetic benchmarks.
Compilation and Synthesis for Fault-Tolerant Digital Microfluidic Biochips (DMBs)

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alistar, M. (Intern)
Number of pages: 1
Publication date: 2014
Event: Poster session presented at 2014 Design, Automation & Test in Europe Conference & Exhibition (DATE), Dresden, Germany.
Main Research Area: Technical/natural sciences
Electronic versions:
DATE_poster.pdf
Source: dtu
Source-ID: u::10993
Publication: Research - peer-review › Poster – Annual report year: 2014

Compilation Tool Chains and Intermediate Representations
In SMECY, we believe that an efficient tool chain could only be defined when the type of parallelism required by an application domain and the hardware architecture is fixed. Furthermore, we believe that once a set of tools is available, it is possible with reasonable effort to change hardware architectures or change the type of parallelism exploited.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Commissariat a l'Energie Atomique, SYLKAN Wild Systems
Authors: Mottin, J. (Ekstern), Pacull, F. (Ekstern), Keryell, R. (Ekstern), Schleuniger, P. (Intern)
Pages: 21-32
Publication date: 2014
Host publication information
Title of host publication: Smart Multicore Embedded Systems
Publisher: Springer
ISBN (Print): 978-1-4614-8799-9
Chapter: 2
Main Research Area: Technical/natural sciences
DOIs:
10.1007/978-1-4614-8800-2_2
Source: FindIt
Source-ID: 2288855834
Publication: Research › Book chapter – Annual report year: 2015
Compiler Feedback using Continuous Dynamic Compilation during Development

Optimizing compilers are vital for performance. However, compilers’ ability to optimize aggressively is limited in some cases. To address this limitation, we have developed a compiler guiding the programmer in making small source code changes, potentially making the source code more amenable to optimization. This tool can help programmers understand what the optimizing compiler has done and suggest automatic source code changes in cases where the compiler refrains from optimizing. We have integrated our tool into an integrated development environment, interactively giving feedback as part of the programmers’ development flow.

We have evaluated our preliminary implementation and show it can guide to a 12% improvement in performance. Furthermore, the tool can be used as an interactive optimization adviser improving the performance of the code generated by a production compiler. Here it can lead to a 153% improvement in performance, indicating the feasibility of the tool as a performance adviser for a production compiler.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Language-Based Technology, Embedded Systems Engineering
Authors: Jensen, N. B. (Intern), Karlsson, S. (Intern), Probst, C. W. (Intern)
Number of pages: 12
Publication date: 2014

Host publication information
Title of host publication: Proceedings - Workshop on Dynamic Compilation Everywhere
Main Research Area: Technical/natural sciences
Workshop: 3rd International Workshop on Dynamic Compilation Everywhere, Vienna, Austria, 21/01/2014
Compiler design, Compiler driven feedback, Automatic refactoring, Automatic vectorization and parallelization
Electronic versions:
Compiler_Feedback.pdf
Source: dtu
Source-ID: u::10751
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Criticality: static profiling for real-time programs

With the increasing performance demand in real-time systems, it becomes more and more important to provide feedback to programmers and software development tools on the performance-relevant code parts of a real-time program. So far, this information was limited to an estimation of the worst-case execution time (WCET) and its associated worst-case execution path (WCEP) only. However, both, the WCET and the WCEP, only provide partial information. Only code parts that are on one of the WCEPs are indicated to the programmer. No information is provided for all other code parts. To give a comprehensive view covering the entire code base, tools in the spirit of program profiling are required.

This work proposes an efficient approach to compute worst-case timing information for all code parts of a program using a complementary metric, called criticality. Every statement of a program is assigned a criticality value, expressing how critical the code is with respect to the global WCET. This gives valuable information about the worst execution path passing through a specific program part compared to the global WCEP. We formally define the criticality metric and investigate some of its properties with respect to dominance in control-flow graphs. Exploiting some of those properties, we propose an algorithm that reduces the overhead of computing the metric to cover complete programs. We also investigate ways to efficiently find only those code parts whose criticality is above a given threshold.

Experiments using well-established real-time benchmark programs show an interesting distribution of the criticality values, revealing considerable amounts of highly critical as well as uncritical code. The metric thus provides ideal information to programmers and software development tools to optimize the worst-case execution time of these programs.

General information
State: Published
Organisations: Embedded Systems Engineering, Department of Applied Mathematics and Computer Science, Vienna University of Technology
Authors: Brandner, F. (Intern), Hepp, S. (Ekstern), Jordan, A. (Ekstern)
Pages: 377-410
Publication date: 2014
Main Research Area: Technical/natural sciences

Publication information
Journal: Real-Time Systems
Volume: 50
Issue number: 3
ISSN (Print): 0922-6443
Ratings:
Decimal Engine for Energy-Efficient Multicore Processors

Prior work demonstrated the use of specialized processors, or accelerators, be energy-efficient for binary floatingpoint (BFP) division and square root, and for decimal floatingpoint (DFP) operations. In the dark silicon era, where not all the circuits on the die can be powered simultaneously, we propose a hybrid BFP/DFP engine to perform BFP division and DFP addition, multiplication and division. The main purpose of this engine is to offload the binary floating-point units for this type of operations and reduce the latency for decimal operations, and power and temperature for the whole die.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
**Design and Implementation of Energy Harvesting Powered Wireless Sensor Networks**

**General information**
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Vuckovic, D. (Intern), Madsen, J. (Intern)
Number of pages: 287
Publication date: 2014

**Publication information**
Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English
Series: DTU Compute PHD-2014
Number: 335
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions:
phd335_Vuckovic_D.pdf
Publication: Research › Ph.D. thesis – Annual report year: 2014

**DySectAPI: Scalable Prescriptive Debugging**

We present the DySectAPI, a tool that allow users to construct probe trees for automatic, event-driven debugging at scale. The traditional, interactive debugging model, whereby users manually step through and inspect their application, does not scale well even for current supercomputers. While lightweight debugging models scale well, they can currently only debug a subset of bug classes. DySectAPI fills the gap between these two approaches with a novel user-guided approach. Using both experimental results and analytical modeling we show how DySectAPI scales and can run with a low overhead on current systems.

**General information**
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Language-Based Technology, Embedded Systems Engineering, Lawrence Livermore National Laboratory, Mesosphere Inc
Authors: Jensen, N. B. (Intern), Karlsson, S. (Intern), Quarfot Nielsen, N. (Ekstern), Lee, G. L. (Ekstern), Ahn, D. H. (Ekstern), Legendre, M. (Ekstern), Schulz, M. (Ekstern)
Number of pages: 1
Publication date: 2014
Event: Poster session presented at International Conference for High Performance Computing, Networking, Storage and Analysis, SC14, New Orleans, United States.
Main Research Area: Technical/natural sciences
Electronic versions:
post237s2_file2.pdf
Links:
Publication: Research - peer-review › Poster – Annual report year: 2014
DySectAPI: Scalable Prescriptive Debugging
We present the DySectAPI, a tool that allow users to construct probe trees for automatic, event-driven debugging at scale. The traditional, interactive debugging model, whereby users manually step through and inspect their application, does not scale well even for current supercomputers. While lightweight debugging models scale well, they can currently only debug a subset of bug classes. DySectAPI fills the gap between these two approaches with a novel user-guided approach. Using both experimental results and analytical modeling we show how DySectAPI scales and can run with a low overhead on current systems.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Language-Based Technology, Embedded Systems Engineering, Lawrence Livermore National Laboratory, Mesosphere Inc
Authors: Jensen, N. B. (Intern), Karlsson, S. (Intern), Quarfot Nielsen, N. (Ekstern), Lee, G. L. (Ekstern), Ahn, D. H. (Ekstern), Legendre, M. (Ekstern), Schulz, M. (Ekstern)
Number of pages: 2
Publication date: 2014
Main Research Area: Technical/natural sciences
Electronic versions:
Extended abstract
Links:
Publication: Research - peer-review › Conference abstract for conference – Annual report year: 2014

Editorial: Thematic series on best articles from IFIPTM and PST

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Malaga
Authors: Fernandez-Gago, C. (Ekstern), Jensen, C. D. (Intern)
Number of pages: 2
Publication date: 2014
Main Research Area: Technical/natural sciences

Publication information
Journal: Journal of Trust Management
Volume: 1
Issue number: 2
ISSN (Print): 2196-064X
Original language: English
Electronic versions:
Editorial.pdf
DOIs:
10.1186/2196-064X-1-2

Bibliographical note
This is an Open Access article distributed under the terms of the Creative Commons Attribution License (http://creativecommons.org/licenses/by/4.0), which permits unrestricted use, distribution, and reproduction in any medium, provided the original work is properly credited
Source: FindIt
Source-ID: 267651513
Publication: Research › Editorial – Annual report year: 2014

Although energy consumption of wireless sensor network has been studied extensively, we are far behind in understanding the dynamics of the power consumption along with energy production using harvesters. We introduce Energy Harvesting Routing Analysis (EHRA) as a formal modelling framework to study wireless sensor networks (WSN) with energy-harvesting capabilities. The purpose of the framework is to analyze WSNs at a high level of abstraction, that is, before the protocols are implemented and before the WSN is deployed. The conceptual basis of EHRA comprises the environment, the medium, computational and physical components, and it captures a broad range of energy-harvesting aware routing protocols. The generic concepts of protocols are captured by a many-sorted signature, and
Concrete routing protocols are specified by corresponding many-sorted algebras. A first analysis tool for EHRA is developed as a simulator implemented using the functional programming language F#. This simulator is used to analyze global properties of WSNs such as network fragmentation, routing trends, and energy profiles for the nodes. Three routing protocols, with a progression in the energy-harvesting awareness, are analyzed on a network that is placed in a heterogeneous environment.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Dung, P. A. (Intern), Hansen, M. R. (Intern), Madsen, J. (Intern)
Pages: 520-540
Publication date: 2014

**Host publication information**

Title of host publication: Specification, Algebra, and Software: Essays Dedicated to Kokichi Futatsugi
Publisher: Springer
ISBN (Print): 978-3-642-54623-5
ISBN (Electronic): 978-3-642-54624-2

Series: Lecture Notes in Computer Science
Volume: 8373
ISSN: 0302-9743
Main Research Area: Technical/natural sciences
DOIs: 10.1007/978-3-642-54624-2_26
Source: dtu
Source-ID: n:oai:DTIC-ART:inspec/445004669::38475
Publication: Research - peer-review › Book chapter – Annual report year: 2014

**ELB-trees - Efficient Lock-free B+trees**

As computer systems scale in the number of processors, data structures with good parallel performance become increasingly important. Lock-free data structures promise improved parallel performance at the expense of higher complexity and sequential execution time. We present ELB-trees, a new lock-free dictionary with simple synchronization in the common case, making it almost 30 times faster than sequential library implementations at 24 threads.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Language-Based Technology, Embedded Systems Engineering
Authors: Bonnichsen, L. F. (Intern), Karlsson, S. (Intern), Probst, C. W. (Intern)
Number of pages: 4
Publication date: 2014
Enabling short fragments for uncoordinated spread spectrum communication

Uncoordinated spread spectrum (USS) protocols have been proposed for anti-jamming communication in wireless settings without shared secrets. The existing USS protocols assume that fragments of hundreds of bits can be transmitted on different channels in order to identify fragments that belong to the same message. However, such long transmissions are susceptible to reactive jamming. To address this problem, we present a protocol that allows the use of short fragments of a few bits only. This makes our scheme resilient to a large class of reactive jammers. We prove that reassembling the fragmented message is not only feasible but also efficient: it can be completed in polynomial time in the size of the message, even if the jammer is computationally resourceful. We demonstrate the protocol efficiency by simulating the reassembly process at the link layer under different design parameters.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Swiss Federal Institute of Technology, Ruhr-University Bochum
Authors: Ahmed, N. (Intern), Pöpper, C. (Ekstern), Capkun, S. (Ekstern)
Pages: 488-507
Publication date: 2014

Energy Efficient FPGA based Hardware Accelerators for Financial Applications

Field Programmable Gate Arrays (FPGAs) based accelerators are very suitable to implement application-specific processors using uncommon operations or number systems. In this work, we design FPGA-based accelerators for two financial computations with different characteristics and we compare the accelerator performance and energy consumption to a software execution of the application. The experimental results show that significant speed-up and energy savings, can be obtained for large data sets by using the accelerator at expenses of a longer development time.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Kenn Toft, J. (Ekstern), Nannarelli, A. (Intern)
Number of pages: 6
Publication date: 2014
Evaluating and Estimating the WCET Criticality Metric

Static analysis tools that are used for worst-case execution time (WCET) analysis of real-time software just provide partial information on an analyzed program. Only the longest-executing path, which currently determines the WCET bound is indicated to the programmer. This limited view can prevent a programmer (or compiler) from targeting optimizations the right way. A possible resort is to use a metric that targets WCET and which can be efficiently computed for all code parts of a program. Similar to dynamic profiling techniques, which execute code with input that is typically expected for the application, based on WCET analysis we can indicate how critical a code fragment is, in relation to the worst-case bound. Computing such a metric on top of static analysis, incurs a certain overhead though, which increases with the complexity of the underlying WCET analysis. We present our approach to estimate the Criticality metric, by relaxing the precision of WCET analysis. Through this, we can reduce analysis time by orders of magnitude, while only introducing minor error. To evaluate our estimation approach and share our garnered experience using the metric, we evaluate real-time programs, which are considered as standard WCET benchmarks. We furthermore demonstrate how the visualization of a Criticality-based profile can aid in the understanding of a program's worst-case behavior.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Jordan, A. (Intern)
Pages: 11-18
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 11th Workshop on Optimizations for DSP and Embedded Systems (ODES '14)
Publisher: Association for Computing Machinery
ISBN (Electronic): 978-1-4503-2595-0
Main Research Area: Technical/natural sciences
Workshop: 11th Workshop on Optimizations for DSP and Embedded Systems (ODES '14), Orlando, United States, 15/02/2014
Criticality, Worst-Case Execution Time, Program Profiling, Program Analysis
DOIs: 10.1145/2568326.2568331
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Evolutionary optimisation of production materials workflow processes

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Department of Management Engineering, Management Science, Production and Service Management
Authors: Herbert, L. T. (Intern), Hansen, Z. N. L. (Intern), Jacobsen, P. (Intern), Cunha, P. (Ekstern)
Publication date: 2014

Host publication information
Title of host publication: Disruptive Innovation in Manufacturing Engineering towards the 4th Industrial Revolution. 8th International Conference on Digital Enterprise Technology - DET 2014
Main Research Area: Technical/natural sciences
Conference: 8th International Conference on Digital Enterprise Technology (DET 2014), Stuttgart, Germany, 25/03/2014 - 25/03/2014
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014
Evolutionary optimization of production materials workflow processes

We present an evolutionary optimisation technique for stochastic production processes, which is able to find improved production materials workflow processes with respect to arbitrary combinations of numerical quantities associated with the production process. Working from a core fragment of the BPMN language, we employ an evolutionary algorithm where stochastic model checking is used as a fitness function to determine the degree of improvement of candidate processes derived from the original process through mutation and cross-over operations. We illustrate this technique using a case study where a baked goods company seeks to improve production time while simultaneously minimising the cost and use of resources.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Department of Management Engineering, Management Science, Production and Service Management
Authors: Herbert, L. T. (Intern), Hansen, Z. N. L. (Intern), Jacobsen, P. (Intern), Cunha, P. (Ekstern)
Pages: 53–60
Publication date: 2014
Conference: 8th International Conference on Digital Enterprise Technology (DET 2014), Stuttgart, Germany, 25/03/2014 - 25/03/2014
BFI conference series: International Conference on Digital Enterprise Technology (5010316)
Main Research Area: Technical/natural sciences

Publication information
Journal: Procedia C I R P
Volume: 25
ISSN (Print): 2212-8271
Ratings:
Scopus rating (2017): SJR 0.668 SNIP 0.982
Scopus rating (2016): CiteScore 1.6 SNIP 1.374 SJR 0.719
Scopus rating (2015): SJR 0.605 SNIP 1.075
Scopus rating (2014): SJR 0.755 SNIP 1.4
Scopus rating (2013): SJR 0.53 SNIP 1.373
ISI indexed (2013): ISI indexed no
Original language: English
Evolutionary algorithm, Stochastic BPMN, Production optimisation
Electronic versions:
Evolutionary_optimization.pdf
DOI:
10.1016/j.procir.2014.10.010
Publication: Research - peer-review › Conference article – Annual report year: 2014

Exposing MPI Objects for Debugging

General information
State: Published
Authors: Brock-Nannestad, L. (Intern), DelSignore, J. (Ekstern), Squyres, J. M. (Ekstern), Karlsson, S. (Intern), Mohror, K. (Ekstern)
Number of pages: 1
Publication date: 2014
Event: Poster session presented at International Conference for High Performance Computing, Networking, Storage and Analysis, SC14, New Orleans, United States.
Main Research Area: Technical/natural sciences
Electronic versions:
laub_sc_14_precropped.pdf
Links:
Source: PublicationPreSubmission
Source-ID: 104278924
Publication: Research - peer-review › Poster – Annual report year: 2014
Exposing MPI Objects for Debugging
Developers rely on debuggers to inspect application state. In applications that use MPI, the Message Passing Interface, the MPI runtime contains an important part of this state. The MPI Tools Working Group has proposed an interface for MPI Handle Introspection. It allows debuggers and MPI implementations to cooperate in extracting information from MPI objects. Information that can then be presented to the developer. MPI Handle Introspection provides a more general interface than previous work, such as Message Queue Dumping.

We add support for introspection to the TotalView debugger and a development version of Open MPI. We explain the interactions between the debugger and MPI library and demonstrate how MPI Handle Introspection raises the abstraction level to simplify debugging of MPI related programming errors.

General information
State: Published
Authors: Brock-Nannestad, L. (Intern), DelSignore, J. (Ekstern), Squyres, J. M. (Ekstern), Karlsson, S. (Intern), Mohror, K. (Ekstern)
Number of pages: 2
Publication date: 2014
Main Research Area: Technical/natural sciences
Electronic versions:
sc_abstract_final.pdf
Links:
Source: PublicationPreSubmission
Source-ID: 104278940
Publication: Research - peer-review Conference abstract for conference – Annual report year: 2014

Guest Editors' Introduction: Special Section on Computer Arithmetic
The articles in this special issue focus on current trends and developments in the field of computer arithmetic. This is a field that encompasses the definition and standardization of arithmetic system for computers. The field also deals with issues of hardware and software implementations and their subsequent testing and verification. Many practitioners of the field also focus on the art and science of using computer arithmetic to carry out scientific and engineering computations. Computer arithmetic is therefore an interdisciplinary field that draws upon mathematics, computer science and electrical engineering. Advances in this field span from being highly theoretical (for instance, new exotic number systems) to being highly practical (for instance, new floating-point units for microprocessors).

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Hawaii, Intel Corporation
Authors: Nannarelli, A. (Intern), Seidel, P. (Ekstern), Tang, P. T. P. (Ekstern)
Number of pages: 2
Pages: 1852-1853
Publication date: 2014
Main Research Area: Technical/natural sciences
Publication information
Journal: I E E E Transactions on Computers
Volume: 63
Issue number: 8
ISSN (Print): 0018-9340
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 2.164 SJR 0.671
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): SJR 0.701 SNIP 2.309 CiteScore 3.42
Hardware Realization of an FPGA Processor - Operating System Call Offload and Experiences

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Hindborg, A. E. (Intern), Karlsson, S. (Intern)
Number of pages: 1
Publication date: 2014
Main Research Area: Technical/natural sciences
Electronic versions:
Hardware Realization of an FPGA Processor - Operating System Call Offload and Experiences

Field-programmable gate arrays, FPGAs, are attractive implementation platforms for low-volume signal and image processing applications. The parallel structure of FPGAs allows for an efficient implementation of parallel algorithms. Sequential algorithms, on the other hand, often perform better on a microprocessor. It is therefore convenient for many applications to employ a synthesizable microprocessor to execute sequential tasks and custom hardware structures to accelerate parallel sections of an algorithm. In this paper, we discuss the hardware realization of Tinuso-I, a small synthesizable processor core that can be integrated in many signal and data processing platforms on FPGAs. We also show how we allow the processor to use operating system services. For a set of SPLASH-2 and SPEC CPU2006 benchmarks we show a speedup of up to 64% over a similar Xilinx MicroBlaze implementation while using 27% to 35% fewer hardware resources.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Hindborg, A. E. (Intern), Karlsson, S. (Intern)
Number of pages: 4
Publication date: 2014

Host publication information
Main Research Area: Technical/natural sciences
Electronic versions:
abstract_ACACES.pdf

Hardware Realization of an FPGA Processor – Operating System Call Offload and Experiences

Field-programmable gate arrays, FPGAs, are attractive implementation platforms for low-volume signal and image processing applications.

The structure of FPGAs allows for an efficient implementation of parallel algorithms. Sequential algorithms, on the other hand, often perform better on a microprocessor. It is therefore convenient for many applications to employ a synthesizable microprocessor to execute sequential tasks and custom hardware structures to accelerate parallel sections of an algorithm. In this paper, we discuss the hardware realization of Tinuso-I, a small synthesizable processor core that can be integrated in many signal and data processing platforms on FPGAs. We also show how we allow the processor to use operating system services. For a set of SPLASH-2 and SPEC CPU2006 benchmarks we show a speedup of up to 64% over a similar Xilinx MicroBlaze implementation while using 27% to 35% fewer hardware resources.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Language-Based Technology
Authors: Hindborg, A. E. (Intern), Schleuniger, P. (Intern), Jensen, N. B. (Intern), Karlsson, S. (Intern)
Number of pages: 8
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 2014 Conference on Design and Architectures for Signal and Image Processing (DASIP)
Publisher: IEEE
Editors: Morawiec, A., Hinderscheit, J.
ISBN (Print): 979-10-92279-05-4
ISBN (Electronic): 979-10-92279-06-1
BFI conference series: Design & Architectures for Signal & Image Processing (5010089)
Main Research Area: Technical/natural sciences
Electronic versions:
Improving Usability of Passphrase Authentication

The combination of user-names and passwords has become the predominant method of user authentication in computer systems. Most users have multiple accounts on different systems, which impose different constraints on the length and complexity of passwords that the user is allowed to select. This is done to ensure an appropriate degree of security, but instead, it makes it difficult for users to remember their password, which results in passwords that are either insecure, but easy to remember, or written down on paper. In this paper we address the problem of usability in user authentication. We promote the use of passphrases, which provide better security and are often easier to remember than passwords. Passphrases will be significantly longer than passwords, which makes them more difficult to enter correctly on a keyboard. We solve this problem by proposing a new passphrase validation algorithm, which accepts the most common typing mistakes. The proposed algorithm has been implemented in secure hardware and integrated into a standard Unix system. We present the design, implementation and preliminary evaluation of the developed passphrase authentication prototype.

General Information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Nielsen, G. (Ekstern), Vedel, M. (Ekstern), Jensen, C. D. (Intern)
Pages: 189-198
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the 2014 Twelfth Annual Conference on Privacy, Security and Trust (PST)
Publisher: IEEE
ISBN (Print): 978-1-4799-3503-1
BFI conference series: Conference on Privacy, Security and Trust (5000610)
Main Research Area: Technical/natural sciences
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

Lazy Spilling for a Time-Predictable Stack Cache: Implementation and Analysis

The growing complexity of modern computer architectures increasingly complicates the prediction of the run-time behavior of software. For real-time systems, where a safe estimation of the program's worst-case execution time is needed, time-predictable computer architectures promise to resolve this problem. A stack cache, for instance, allows the compiler to efficiently cache a program's stack, while static analysis of its behavior remains easy. Likewise, its implementation requires little hardware overhead.

This work introduces an optimization of the standard stack cache to avoid redundant spilling of the cache content to main memory, if the content was not modified in the meantime. At first sight, this appears to be an average-case optimization. Indeed, measurements show that the number of cache blocks spilled is reduced to about 17% and 30% in the mean, depending on the stack cache size. Furthermore, we show that lazy spilling can be analyzed with little extra effort, which benefits the worst-case spilling behavior that is relevant for a real-time system.

General Information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, ENSTA ParisTech
Authors: Abbaspourseyedi, S. (Intern), Jordan, A. (Intern), Brandner, F. (Ekstern)
Number of pages: 10
Pages: 83-92
Publication date: 2014

Host publication information
Title of host publication: Proceedings of 14th International Workshop on Worst-Case Execution Time Analysis : WCET 2014
Publisher: OASICS
Editor: Falk, H.
ISBN (Electronic): 978-3-939897-69-9
Series: Open Access Series in Informatics
Volume: 39
Library Support for Resource Constrained Accelerators

Accelerators, and other resource constrained systems, are increasingly being used in computer systems. Accelerators provide power efficient performance and often provide a shared memory model. However, it is a challenge to map feature rich APIs, such as OpenMP, to resource constrained systems. In this paper, we present a lightweight system where an accelerator can remotely execute library functions on a host processor. The implementation takes up 750 bytes but can replace arbitrary library calls leading to significant savings in memory footprint. We evaluate with a set of SPLASH-2 applications and show that the impact on execution time is negligible when compared to GCC’s OpenMP implementation.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Brock-Nannestad, L. (Intern), Karlsson, S. (Intern)
Pages: 187-201
Publication date: 2014
**Medium Access Control in Energy Harvesting - Wireless Sensor Networks**

Focusing on Wireless Sensor Networks (WSN) that are powered by energy harvesting, this dissertation focuses on energy-efficient communication links between senders and receivers that are alternating between active and sleeping states of operation. In particular, the focus lies on Medium Access Control (MAC) protocols that are following the receiver-initiated paradigm of asynchronous communication. According to the receiver-initiated paradigm the communication is initiated by the receiver that states its availability to receive data through beacons. The sender is passively listening to the channel until it receives the beacon of interest.

In this context, the dissertation begins with an in-depth survey of all the receiver-initiated MAC protocols and presents their unique optimization features, which deal with several challenges of the link layer such as mitigation of the energy consumption, collision avoidance, provision of Quality of Service (QoS) and security. Focusing on the particular requirements of an energy harvesting application, the dissertation continues with the presentation of a MAC protocol, named ODMAC, which extends the receiver-initiated paradigm with several energy-efficient features that aim to adapt the consumed energy to match the harvested energy, distribute the load with respect to the harvested energy, decrease the overhead of the communication, address the requirements for collision avoidance, prioritize urgent traffic and secure the system against beacon replay attacks.

The performance and behavior of ODMAC and its features are compared to the state-of-the-art and evaluated using mathematical models, simulations and testbed experiments that are based on eZ430-rf2500 wireless development platform. The results validate the efficient use of the harvested energy and demonstrate sustainable operation.

---

**MPI Debugging with Handle Introspection**

The Message Passing Interface, MPI, is the standard programming model for high performance computing clusters. However, debugging applications on large scale clusters is difficult. The widely used Message Queue Dumping interface enables inspection of message queue state but there is no general interface for extracting information from MPI objects such as communicators. A developer can debug the MPI library as if it was part of the application, but this exposes an unneeded level of detail.

The Tools Working Group in the MPI Forum has proposed a specification for MPI Handle Introspection. It defines a standard interface that lets debuggers extract information from MPI objects. Extracted information is then presented to the developer, in a human readable format. The interface is designed to be independent of MPI implementations and debuggers.

In this paper, we describe our support for introspection in the TotalView debugger and test it against a reference introspection implementation in Open MPI. We also describe how the debugger interfaces with the MPI implementation.

---

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Fafoutis, X. (Intern), Dragoni, N. (Intern), Madsen, J. (Intern)
Number of pages: 222
Publication date: 2014

**Publication information**
Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English

Series: DTU Compute PHD-2014
Number: 328
ISSN: 0909-3192
Main Research Area: Technical/natural sciences

**Electronic versions:**
phd328_Fafoutis_X.pdf
Publication: Research › Ph.D. thesis – Annual report year: 2014

---

**General information**

State: Published
Authors: Brock-Nannestad, L. (Intern), DelSignore, J. (Ekstern), Squyres, J. M. (Ekstern), Karlsson, S. (Intern), Mohror, K. (Ekstern)
Number of pages: 4
Publication date: 2014

Event: Paper presented at Workshop on Exascale MPI (ExaMPI 2014), New Orleans, United States.
Main Research Area: Technical/natural sciences
Online Synthesis for Operation Execution Time Variability on Digital Microfluidic Biochips
Several approaches have been proposed for the synthesis of digital microfluidic biochips, which, starting from a biochemical application and a given biochip architecture, determine the allocation, resource binding, scheduling, placement and routing of the operations in the application. Researchers have assumed that each biochemical operation in an application is characterized by a worst-case execution time (wcet). However, during the execution of the application, due to variability and randomness in biochemical reactions, operations may finish earlier than their wcets. In this paper we propose an online synthesis strategy that re-synthesizes the application at runtime when operations experience variability in their execution time, obtaining thus shorter application execution times. The proposed strategy has been evaluated using several benchmarks.

Open Core Protocol (OCP) Clock Domain Crossing Interfaces
The open core protocol (OCP) is an openly licensed configurable and scalable interface protocol for on-chip subsystem communications. The protocol defines read and write transactions from a master towards a slave across a point-to-point connection and the protocol assumes a single common clock. This paper presents the design of two OCP clock domain crossing interface modules that can be used to construct systems with multiple clock domains. An OCP interface typically has control signals related to both the master issuing a read or write request and the slave producing a response. If all these control signals are passed across the clock-domain boundary and synchronized it may add significant latency to the duration of a transaction. Our interface designs avoid this and synchronize only a single signal transition in each direction during a read or a write transaction.

While the problem of synchronizing a simple streaming interface is well described in the literature and often solved using bi-synchronous FIFOs we found surprisingly little published material addressing synchronization of bus-style read-write transaction interfaces.
Optimization of Partitioned Architectures to Support Soft Real-Time Applications
In this paper we propose a new Tabu Search-based design optimization strategy for mixed-criticality systems implementing hard and soft real-time applications on the same platform. Our proposed strategy determined an implementation such that all hard real-time applications are schedulable and the quality of service of the soft real-time tasks is maximized. We have evaluated our strategy using an aerospace case study.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering
Authors: Tamas-Selicean, D. (Intern), Pop, P. (Intern)
Number of pages: 2
Pages: 223 - 224
Publication date: 2014

Optimization of TTEthernet Networks to Support Best-Effort Traffic
This paper focuses on the optimization of the TTEthernet communication protocol, which offers three traffic classes: time-triggered (TT), sent according to static schedules, rate-constrained (RC) that has bounded end-to-end latency, and best-effort (BE), the classic Ethernet traffic, with no timing guarantees. In our earlier work we have proposed an optimization approach named DOTTTS that performs the routing, scheduling and packing / fragmenting of TT and RC messages, such that the TT and RC traffic is schedulable. Although backwards compatibility with classic Ethernet networks is one of TTEthernet’s strong points, there is little research on this topic. However, in this paper, we extend our DOTTTS optimization approach to optimize TTEthernet networks, such that not only the TT and RC messages are schedulable, but we also maximize the available bandwidth for BE messages. The proposed optimization has been evaluated on a space application case study.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science , Embedded Systems Engineering
Authors: Tamas-Selicean, D. (Intern), Pop, P. (Intern)
Pages: 1-4
Publication date: 2014
Performance Aspects of Synthesizable Computing Systems

Embedded systems are used in a broad range of applications that demand high performance within severely constrained mechanical, power, and cost requirements. Embedded systems implemented in ASIC technology tend to provide the highest performance, lowest power consumption and lowest unit cost. However, high setup and design costs make ASICs economically viable only for high volume production. Therefore, FPGAs are increasingly being used in low and medium volume markets. The evolution of FPGAs has reached a point where multiple processor cores, dedicated accelerators, and a large number of interfaces can be integrated on a single device.

This thesis consists of five parts that address performance aspects of synthesizable computing systems on FPGAs. First, it is evaluated how synthesizable processor cores can exploit current state-of-the-art FPGA architectures. This evaluation results in a processor architecture optimized for a high throughput on modern FPGA architectures. The current hardware implementation, the Tinuso I core, can be clocked as high as 376MHz on a Xilinx Virtex 6 device and consumes fewer hardware resources than similar commercial processor configurations. The Tinuso architecture leverages predicated execution to circumvent costly pipeline stalls due to branches and exposes hazards to the compiler to keep the hardware simple. Second, it is investigated if a production compiler, GCC, is able to successfully leverage predicated execution and schedule instructions so as to mitigate the hazards. The third part of this thesis describes the design and implementation of communication structures for Tinuso multicore configurations and evaluates the scalability of these systems. Forth, a case study shows how to map a high performance synthetic aperture radar application to a synthesizable multicore system. The proposed system includes 64 processor cores and a 2D mesh interconnect on a single FPGA device and consumes about 10 watt only. Finally, a task based programming model is proposed that allows for easily expressing parallelism and simplifies memory management.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schleuniger, P. (Intern), Karlsson, S. (Intern), Madsen, J. (Intern)
Number of pages: 213
Publication date: 2014

Publication information
Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English
Series: DTU Compute PHD-2014
Number: 337
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions:
Performance_Aspects_of.pdf
Publication: Research › Ph.D. thesis – Annual report year: 2014

Programming language and tools for Multipurpose Lab-on-a-Chip Platforms

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Department of Chemical and Biochemical Engineering, Center for Process Engineering and Technology, Technical University of Denmark
Authors: Pop, P. (Intern), Madsen, J. (Intern), Understrup, K. (Ekstern), Alistar, M. (Intern), Minhass, W. H. (Intern), Krühne, U. (Intern)
Number of pages: 1
Publication date: 2014
Event: Poster session presented at 6th Annual Lab-on-a-Chip European Congress, Berlin, Germany.
Remote Biometrics for Robust Persistent Authentication

This paper examines the problem of providing a robust non-invasive authentication service for mobile users in a smart environment. We base our work on the persistent authentication model (PAISE), which relies on available sensors to track principals from the location where they authenticate, e.g., through a smart card based access control system, to the location where the authentication is required by a location-based service. The PAISE model is extended with remote biometrics to prevent the decay of authentication confidence when authenticated users encounter and interact with other users in the environment. The result is a calm approach to authentication, where mobile users are transparently authenticated towards the system, which allows the provision of location-based services. The output of the remote biometrics are fused using error-rate-based fusion to solve a common problem that occurs in score level fusion, i.e., the scores of each biometric system are usually incompatible, as they have different score ranges as well as different probability distributions.

We have integrated remote biometrics with the PAISE prototype and the experimental results on a publicly available dataset, show that fusion of two remote biometric modalities, facial recognition and appearance analysis, gives a significant improvement over each of the individual experts. Furthermore, the experimental results show that using remote biometrics increases the performance of tracking in persistent authentication, by identifying principals who are difficult to track due to occlusions in crowded scenes.

Resilient Infrastructure and Building Security

Traditional authentication systems are considered persistent as they rarely limit the time the authentication is valid. Conversely, sensor-based authentication systems are considered transient as they allow continuous authentication of the users.

In this thesis we present a new approach to authentication that combines traditional access control systems with the sensing technologies and tracking capabilities offered by smart environments. Our approach is called Persistent Authentication for Location-based Services. Persistent authentication enables the secure provision of location-based services through non-intrusive authentication of mobile users in a smart environment. The objective is to shift the current authentication paradigm from a single discrete event to a continuous session. This is accomplished by utilising the contextual awareness provided by the smart environment to track principals from the point of initial authentication to the
point where authorisation is requested by location-based services.

Facial recognition and appearance analysis are integrated in the persistent authentication system as remote biometric experts that operate at a distance and require no interaction from the users. The experts perform continuous authentication by processing samples of the biometric modalities as they become available.

Combining scores from multiple biometric experts is known as sensor fusion. A common challenge in this field is that the results from evaluating different biometric characteristic are usually incompatible, as they have different score ranges as well as different probability distributions. Error-rate-based fusion is presented as a novel fusion technique that transforms individual scores from different biometric systems into objective evidences and combine them using Bayesian inference.

Persistent authentication offers an effective integrated protection measure that is distributed directly in the facility and is non-intrusive to the public and affordable to the facility owners. Persistent authentication is suitable for security sensitive applications and can help protect the facility against terrorism and other types of crime.
Safe Asynchronous System Calls

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Brock-Nannestad, L. (Intern), Karlsson, S. (Intern)
Number of pages: 1
Publication date: 2014
Main Research Area: Technical/natural sciences
Electronic versions:
cgo_poster_laub.pdf

Bibliographical note
Poster at the CGO2014 ACM Student Research Competition (SRC).
Source: PublicationPreSubmission
Source-ID: 102283566
Publication: Research - peer-review › Poster – Annual report year: 2014

Safe Asynchronous System Calls - extended abstract

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Brock-Nannestad, L. (Intern), Karlsson, S. (Intern)
Number of pages: 4
Publication date: 2014
Main Research Area: Technical/natural sciences
Electronic versions:
cgo_abstract.pdf

Bibliographical note
Extended abstract for poster at the CGO2014 ACM Student Research Competition (SRC).
Source: PublicationPreSubmission
Source-ID: 102283572
Publication: Research - peer-review › Conference abstract for conference – Annual report year: 2014

Safety-Critical Java for Embedded Systems

Safety-critical systems are real-time systems whose failure can have severe or catastrophic consequences, possibly endangering human life. Many safety-critical systems incorporate embedded computers used to control different tasks. Software running on safety-critical systems needs to be certified before its deployment and the most time-consuming step of this process is the testing and verification phase. Due to the increasing complexity in safety-critical systems there is a need for new technologies that can facilitate testing and verification activities. The safety-critical specification for Java aims at providing a reduced set of the Java programming language that can be used for systems that need to be certified at the highest levels of criticality. Safety-critical Java (SCJ) restricts how a developer can structure an application by providing a specific programming model and by restricting the set of methods and libraries that can be used. Furthermore, its memory model do not use a garbage-collected heap but scoped memories.

In this thesis we examine the use of the SCJ specification through an implementation in a time-predictable, FPGA-based Java processor. The specification is now in a mature state and with our implementation we have proved its feasibility in an embedded platform. Moreover, we have explored how simple hardware extensions can reduce the execution time of time-critical operations required by the SCJ specification.

The scoped memory model used in SCJ is perhaps one of its most difficult features to use correctly. Therefore, in this work we have also studied practical aspects of its usage by developing scoped memory use patterns and reusable libraries aiming at facilitating the development of complex software systems.
SBAT. A stochastic BPMN analysis tool

This paper presents SBAT, a tool framework for the modelling and analysis of complex business workflows. SBAT is applied to analyse an example from the Danish baked goods industry.

Based upon the Business Process Modelling and Notation (BPMN) language for business process modelling, we describe a formalised variant of this language extended to support the addition of intention preserving stochastic branching and parameterised reward annotations. Building on previous work, we detail the design of SBAT, a software tool which allows for the analysis of BPMN models. Within SBAT, properties of interest are specified using the temporal logic Probabilistic Computation Tree Logic (PCTL) and we employ stochastic model checking, by means of the model checker PRISM, to compute their exact values.

We present a simplified example of a distributed stochastic system where we determine a reachability property and the value of associated rewards in states of interest for a real-world example from a case company in the Danish baked goods industry. The developments are presented in a generalised fashion to make them relevant to the general problem of implementing quantitative probabilistic model checking of graph-based process modelling languages.

This paper contains three key elements:
1. SBAT description.
2. Case company description.

The paper concludes by indicating SBAT’s practical applicability and suggests further research directions.
SBOAT: A Stochastic BPMN Analysis and Optimisation Tool

In this paper we present a description of a tool development framework, called SBOAT, for the quantitative analysis of graph based process modelling languages based upon the Business Process Modelling and Notation (BPMN) language, extended with intention preserving stochastic branching and parameterised reward annotations. SBOAT allows the optimisation of these processes by specifying optimisation goals by means of probabilistic control tree logic (PCTL). Optimisation is performed by means of an evolutionary algorithm where stochastic model checking, in the form of the PRISM model checker, is used to compute the fitness, the performance of a candidate in terms of the specified goals, of variants of a process. Our evolutionary algorithm approach uses a matrix representation of process models to efficiently allow mutation and crossover of a process model to be performed, allowing broad exploration of the space of possible models.

We present a simple example of a distributed stochastic system where we determine a reachability property and the value of associated rewards in states of interest for a generated range of models. This example is taken from a case company in the Danish baking industry and will illustrate the practical applicability of this tool by helping the company analyse and optimise selected workflows.

Scope-Based Method Cache Analysis

The quest for time-predictable systems has led to the exploration of new hardware architectures that simplify analysis and reasoning in the temporal domain, while still providing competitive performance. For the instruction memory, the method cache is a conceptually attractive solution, as it requests memory transfers at well-defined instructions only. In this article, we present a new cache analysis framework that generalizes and improves work on cache persistence analysis. The analysis demonstrates that a global view on the cache behavior permits the precise analyses of caches which are hard to analyze by inspecting cache state locally.
Security and Privacy in Video Surveillance: Requirements and Challenges

Use of video surveillance has substantially increased in the last few decades. Modern video surveillance systems are equipped with techniques that allow traversal of data in an effective and efficient manner, giving massive powers to operators and potentially compromising the privacy of anyone observed by the system. Several techniques to protect the privacy of individuals have therefore been proposed, but very little research work has focused on the specific security requirements of video surveillance data (in transit or in storage) and on authorizing access to this data. In this paper, we present a general model of video surveillance systems that will help identify the major security and privacy requirements for a video surveillance system and we use this model to identify practical challenges in ensuring the security of video surveillance data in all stages (in transit and at rest). Our study shows a gap between the identified security requirements and the proposed security solutions where future research efforts may focus in this domain.
**Smart Multicore Embedded Systems**

This book provides a single-source reference to the state-of-the-art of high-level programming models and compilation tool-chains for embedded system platforms. The authors address challenges faced by programmers developing software to implement parallel applications in embedded systems, where very often they are forced to rewrite sequential programs into parallel software, taking into account all the low level features and peculiarities of the underlying platforms. Readers will benefit from these authors’ approach, which takes into account both the application requirements and the platform specificities of various embedded systems from different industries. Parallel programming tool-chains are described that take as input parameters both the application and the platform model, then determine relevant transformations and mapping decisions on the concrete platform, minimizing user intervention and hiding the difficulties related to the correct and efficient use of memory hierarchy and low level code generation.

Describes tools and programming models for multicore embedded systems Emphasizes throughout performance per watt scalability Discusses realistic limits of software parallelization Enables software migration from single to multi-core Includes coverage of fault-tolerance and dynamic reconfiguration Uses case studies to demonstrate techniques presented

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Pisa, Delft University of Technology, Commisariat Energie Atomique
Authors: Torquati, M. (ed.) (Ekstern), Bertels, K. (ed.) (Ekstern), Karlsson, S. (ed.) (Intern), Pacull, F. (ed.) (Ekstern)
Number of pages: 175
Publication date: 2014

**Publication information**

Publisher: Springer
ISBN (Print): 978-1-4614-8799-9
Original language: English
Main Research Area: Technical/natural sciences
DOIs: 10.1007/978-1-4614-8800-2
Publication: Research - peer-review › Book – Annual report year: 2014

**Specification, Verification and Optimisation of Business Processes: A Unified Framework**

This thesis develops a unified framework wherein to specify, verify and optimise stochastic business processes.

This framework provides for the modelling of business processes via a mathematical structure which captures business processes as a series of connected activities. This structure is extended with stochastic branching, message passing and reward annotations which allow for the modelling of resources consumed during the execution of a business process. Further, it is shown how this structure can be used to formalise the established business process modelling language Business Process Model and Notation (BPMN).

The automated analysis of business processes is done by means of quantitative probabilistic model checking which allows verification of validation and performance properties through use of an algorithm for the translation of business process models into a format amenable to model checking. This allows for a rich set of both qualitative and quantitative properties of a business process to be precisely determined in an automated fashion directly from the model of the business process.

A number of advanced applications of this framework are presented which allow for automated fault tree analysis and the automated optimisation of business processes by means of an evolutionary algorithm.

This work is motivated by problems that stem from the healthcare sector, and examples encountered in this field are used to illustrate these developments.

**General information**

State: Published
Synthesis and Layout of an Asynchronous Network-on-Chip using Standard EDA Tools

Asynchronous circuit design is well understood but design tools supporting asynchronous design are largely lacking, and designers are limited to using conventional EDA-tools. These tools have a built-in synchronous mind-set and this complicates their use for asynchronous implementation. One example is the key role that clock signals play in specifying time-constraints for the synthesis. In this paper explain how we handled the synthesis and layout of an asynchronous network-on-chip for a multi-core platform. Focus is on the design process while the actual NOC-design and its performance are presented elsewhere.

T-Crest: A Time-Predictable Multi-Core Platform For Aerospace Applications

Space systems are hard real-time systems, where the worst-case execution time (WCET) of tasks needs to be known to prove absence of deadline misses. For simple processor and memory architectures it is possible to statically derive a safe upper bound of the WCET. However, future requirements in more autonomous missions require more processing power. This increase in processing power is approached by multi-core processors. However, current multi-core processors are not WCET analyzable. The mission of T-CREST is to develop tools and build a multi-core system that provides high performance, but be WCET analyzable. The T-CREST time-predictable system will simplify the safety argument with respect to the maximum execution time and increase the performance with multi-core technology. Thus the T-CREST system will result in lower costs for safety-relevant applications, reducing system complexity, simultaneously providing faster time-predictable execution. Most of the T-CREST technology is available in open-source.
Testing Infrastructure for Operating System Kernel Development

Testing is an important part of system development, and to test effectively we require knowledge of the internal state of the system under test. Testing an operating system kernel is a challenge as it is the operating system that typically provides access to this internal state information. Multi-core kernels pose an even greater challenge due to concurrency and their shared kernel state. In this paper, we present a testing framework that addresses these challenges by running the operating system in a virtual machine, and using virtual machine introspection to both communicate with the kernel and obtain information about the system. We have also developed an in-kernel testing API that we can use to develop a suite of unit tests in the kernel. We are using our framework for the development of our own multi-core research kernel.

The importance of trust in computer security

The computer security community has traditionally regarded security as a "hard" property that can be modelled and formally proven under certain simplifying assumptions. Traditional security technologies assume that computer users are either malicious, e.g. hackers or spies, or benevolent, competent and well informed about the security policies. Over the past two decades, however, computing has proliferated into all aspects of modern society and the spread of malicious software (malware) like worms, viruses and botnets have become an increasing threat. This development indicates a failure in some of the fundamental assumptions that underpin existing computer security technologies and that a new view of computer security is long overdue.

In this paper, we examine traditional models, policies and mechanisms of computer security in order to identify areas where the fundamental assumptions may fail. In particular, we identify areas where the "hard" security properties are based on trust in the different agents in the system and certain external agents who enforce the legislative and contractual frameworks.

Trust is generally considered a "soft" security property, so building a "hard" security mechanism on trust will at most give a spongy result, unless the underlying trust assumptions are made first class citizens of the security model. In most of the work in computer security, trust assumptions are implicit and they will surely fail when the environment of the systems change, e.g. when systems are used on a global scale on the Internet. We argue that making such assumptions about trust explicit is an essential requirement for the future of system security and argue why the formalisation of computational
trust is necessary when we wish to reason about system security.

Tradeoff analysis for Dependable Real-Time Embedded Systems during the Early Design Phases

Embedded systems are becoming increasingly complex and have tight competing constraints in terms of performance, cost, energy consumption, dependability, flexibility, security, etc. The objective of this thesis is to propose design methods and tools for supporting the tradeoff analysis of competing design objectives during the early design phases, which are characterized by uncertainties. We consider safety-critical real-time applications modeled as task graphs, to be implemented on distributed heterogeneous architectures consisting of processing elements (PEs), interconnected by a shared communication channel. Tasks are scheduled using fixed-priority preemptive scheduling, and we use non-preemptive scheduling for messages.

As a first step, we address the problem of function-to-task decomposition. In this context we have assumed that the application functionality is captured by a set of functional blocks, with different safety requirements. We propose a Genetic Algorithm-based metaheuristic to solve the function-to-task decomposition problem. Our algorithm also decides the mapping of tasks to the PEs of a distributed architecture and the reliability of each PE in the architecture, such that the safety and integrity constraints are satisfied, the schedulability of the real-time application is guaranteed and the overall development and product unit costs are minimized.

Next, we investigate tradeoffs between performance, energy and reliability. Addressing energy and reliability simultaneously is especially challenging, since lowering the voltage to reduce the energy consumption has been shown to increase the transient fault rate. We are interested to tolerate transient faults and we use task replication for recovery. We propose a Tabu Search-based approach, which decides the mapping of tasks to processing elements, as well as the processor voltage and frequency levels for executing each task, such that transient faults are tolerated, the real-time constraints of the application are satisfied, and the energy consumed is minimized.

In this thesis, we target the early design phases, when decisions have a high impact on the subsequent implementation choices. However, due to a lack of information, the early design phases are characterized by uncertainties, e.g., in the worst-case execution times (WCETs), in the functionality requirements, or in the hardware component costs. In this context, we select the hardware components for the architecture and derive a mapping of tasks in the application, such that the resulted implementation is both robust and flexible. The architecture also has a high chance to have its unit cost within the cost budget. Robust means that the application has a high chance of being schedulable, considering the WCET uncertainties, whereas a flexible mapping has a high chance to successfully accommodate future functionality changes. We propose a Genetic Algorithm-based approach to solve this optimization problem. The proposed tradeoff analysis methods have been evaluated using several synthetic and real-life benchmarks.
Twenty Years of Research on RNS for DSP: Lessons Learned and Future Perspectives

In this paper, we discuss a number of issues emerged from our twenty-year long experience in applying the Residue Number System (RNS) to DSP systems. In early days, RNS was mainly used to reach the maximum performance in speed. Today, RNS is also used to obtain power-efficient (tradeoffs speed-power) and reliable systems (redundant RNS). Advances in microelectronics and CAD tools play an important role in favoring one technology over another, and a winning choice of the past may become at disadvantage today. In this paper, we address a number of factors influencing the choice of RNS as the winning solution. From technology platforms (ASIC and FPGA), to issue related to modern design tools, from cost of memory, to cost of wiring, from power dissipation to thermal issues. Moreover, we mention how RNS can be helpful in implementing reliable architectures (fault detection and correction) in future VLSI systems.
Unit Testing Framework for Operating System Kernels

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Walter, M. (Intern), Karlsson, S. (Intern)
Number of pages: 1
Publication date: 2014
Event: Poster session presented at 11th USENIX Symposium on Operating Systems Design and Implementation (OSDI '14), Broomfield, United States.
Main Research Area: Technical/natural sciences

Using quantitative stochastic model checking tool to increase safety and improve efficiency in production processes

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Department of Management Engineering, Management Science
Authors: Herbert, L. T. (Intern), Hansen, Z. N. L. (Intern), Jacobsen, P. (Intern)
Pages: 2405-2416
Publication date: 2014

Host publication information
Title of host publication: Proceedings of the European Safety and Reliability Conference ESREL 2014
Publisher: CRC Press
ISBN (Print): 9781138026810
BFI conference series: European Safety and Reliability conference (5010077)
Main Research Area: Technical/natural sciences
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

WCET-based comparison of an instruction scratchpad and a method cache
This paper compares two proposed alternatives to conventional instruction caches: a scratchpad memory (SPM) and a method cache. The comparison considers the true worst-case execution time (WCET) and the estimated WCET bound of programs using either an SPM or a method cache, using large numbers of randomly generated programs. For these programs, we find that a method cache is preferable to an SPM if the true WCET is used, because it leads to execution times that are no greater than those for SPM, and are often lower. However, we also find that analytical pessimism is a significant problem for a method cache. If WCET bounds are derived by analysis, the WCET bounds for an instruction SPM are often lower than the bounds for a method cache. This means that an SPM may be preferable in practical systems.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of York
Authors: Whitham, J. (Ekstern), Schoeberl, M. (Intern)
Pages: 301-308
Publication date: 2014

Host publication information
Title of host publication: 2014 IEEE 17th International Symposium on Object/Component/Service-Oriented Real-Time Distributed Computing (ISORC)
Publisher: IEEE
Editor: O'Connor, L.
Workflow Fault Tree Generation Through Model Checking

We present a framework for the automated generation of fault trees from models of real-world process workflows, expressed in a formalised subset of the popular Business Process Modelling and Notation (BPMN) language. To capture uncertainty and unreliability in workflows, we extend this formalism with probabilistic non-deterministic branching. We present an algorithm that allows for exhaustive generation of possible error states that could arise in execution of the model, where the generated error states allow for both fail-stop behaviour and continued system execution. We employ stochastic model checking to calculate the probabilities of reaching each non-error system state. Each generated error state is assigned a variable indicating its individual probability of occurrence. Our method can determine the probability of combined faults occurring, while accounting for the basic probabilistic structure of the system being modelled. From these calculations, a comprehensive fault tree is generated. Further, we show that annotating the model with rewards (data) allows the expected mean values of reward structures to be calculated at points of failure.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Herbert, L. T. (Intern), Sharp, R. (Intern)
Pages: 2229-2236
Publication date: 2014

Host publication information
Title of host publication: Safety, Reliability and Risk Analysis: Beyond the Horizon: Proceedings
Publisher: CRC Press
Editors: Steenbergen, R., van Gelder, P., Miraglia, S., Ton Vrouwenvelder, A.
ISBN (Print): 978-1-138-00123-7
Main Research Area: Technical/natural sciences
Conference: 22nd ESREL conference, Amsterdam, Netherlands, 30/09/2013 - 30/09/2013
BPMN, Stochastic BPMN, Stochastic Model Checking, Quantitative Model Checking, Formal Risk Analysis, Fault Tree Analysis, Fault Tree Generation
Electronic versions:
Workflow_Fault_Tree_Generation.pdf

Bibliographical note
22nd ESREL conference, Amsterdam, 30 September - 2 October 2013.
Source: dtu
Source-ID: u:9448
Publication: Research - peer-review › Article in proceedings – Annual report year: 2014

A 65-nm CMOS Area Optimized De-synchronization Flow for sub-VT Designs
This paper proposes a process independent post layout de-synchronization flow implemented in tool command language working on designs operating in the sub-VT regime. The overhead due to the self-timed operation is combated by introducing full-custom delay elements and latches for a standard 65-nm CMOS process. The flow offers the possibility to adjust granularity based on user requirements. Case studies with different reference designs manifested an average
A Behavioral Study on the Effects of Rock Music on Auditory Attention

We are interested in the distribution of top-down attention in noisy environments, in which the listening capability is challenged by rock music playing in the background. We conducted behavioral experiments in which the subjects were asked to focus their attention on a narrative and detect a specific word, while the voice of the narrator was masked by rock songs that were alternating in the background. Our study considers several types of songs and investigates how their distinct features affect the ability to segregate sounds. Additionally, we examine the effect of the subjects' familiarity to the music.

Analyzing Properties of Stochastic Business Processes By Model Checking

This chapter presents an approach to precise formal analysis of business processes with stochastic properties. The method presented here allows for both qualitative and quantitative properties to be individually analyzed at design time without requiring a full specification. This provides an effective means to explore possible designs for a business process and to debug any flaws.
An area-efficient network interface for a TDM-based Network-on-Chip

Network interfaces (NIs) are used in multi-core systems where they connect processors, memories, and other IP-cores to a packet switched Network-on-Chip (NOC). The functionality of a NI is to bridge between the read/write transaction interfaces used by the cores and the packet-streaming interface used by the routers and links in the NOC. The paper addresses the design of a NI for a NOC that uses time division multiplexing (TDM). By keeping the essence of TDM in mind, we have developed a new area-efficient NI micro-architecture. The new design completely eliminates the need for FIFO buffers and credit based flow control - resources which are reported to account for 50–85% of the area in existing NI designs. The paper discusses the design considerations, presents the new NI micro-architecture, and reports area figures for a range of implementations.

A network-flow based valve-switching aware binding algorithm for flow-based microfluidic biochips

Designs of flow-based microfluidic biochips are receiving much attention recently because they replace conventional biological automation paradigm and are able to integrate different biochemical analysis functions on a chip. However, as the design complexity increases, a flow-based microfluidic biochip needs more chip-integrated micro-valves, i.e., the basic unit of fluid-handling functionality, to manipulate the fluid flow for biochemical applications. Moreover, frequent switching of micro-valves results in decreased reliability. To minimize the valve-switching activities, we develop a network-flow based resource binding algorithm based on breadth-first search (BFS) and minimum cost maximum flow (MCMF) in architectural-level synthesis. The experimental results show that our methodology not only makes significant reduction of valve-switching activities but also diminishes the application completion time for both real-life applications and a set of synthetic benchmarks.
An SDRAM controller for real-time systems

For real-time systems we need to statically determine worst-case execution times (WCET) of tasks to proof the schedulability of the system. To enable static WCET analysis, the platform needs to be time-predictable. The platform includes the processor, the caches, the memory system, the operating system, and the application software itself. All those components need to be timing analyzable. Current computers use DRAM as a cost effective main memory. However, these DRAM chips have timing requirements that depend on former accesses and also need to be refreshed to retain their content. Standard memory controllers for DRAM memories are optimized to provide maximum bandwidth or throughput at the cost of variable latency for individual memory accesses. In this paper we present an SDRAM controller for realtime systems. The controller is optimized for the worst case and constant latency to provide a base of the memory hierarchy for time-predictable systems.

Application-specific fault-tolerant architecture synthesis for digital microfluidic biochips

Microfluidic-based biochips are replacing the conventional biochemical analyzers, and are able to integrate onchip all the necessary functions for biochemical analysis using microfluidics. The digital microfluidic biochips are based on the manipulation of liquids not as a continuous flow, but as discrete droplets on an array of electrodes. Microfluidic operations, such as transport, mixing, split, are performed on this array by routing the corresponding droplets on a series of electrodes. Researchers have proposed several approaches for the synthesis of digital microfluidic biochips. All previous
work assumes that the biochip architecture is given, and most approaches consider a rectangular shape for the electrode array. However, non-regular application-specific architectures are common in practice. Hence, in this paper, we propose an approach to the application-specific architecture synthesis. Our approach can also help the designer to increase the yield by introducing redundant electrodes to tolerate permanent faults. The proposed architecture synthesis algorithm has been evaluated using several benchmarks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alistar, M. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Pages: 794-800
Publication date: 2013

Host publication information
Title of host publication: Proceedings of the 18th Asia and South Pacific Design Automation Conference (ASP-DAC)
ISBN (Print): 9781467330299
BFI conference series: Asia and South Pacific Design Automation Conference (5000305)
Main Research Area: Technical/natural sciences
Conference: 18th Asia and South Pacific Design Automation Conference (ASP-DAC 2013), Yokohama, Japan, 22/01/2013 - 22/01/2013
DOIs: 10.1109/ASPDAC.2013.6509697
Source: dtu
Source-ID: n:oai:DTIC-ART:iel/385918898::28294
Publication: Research - peer-review > Article in proceedings – Annual report year: 2013

ASAM: Automatic architecture synthesis and application mapping
This paper focuses on mastering the automatic architecture synthesis and application mapping for heterogeneous massively-parallel MPSoCs based on customizable application-specific instruction-set processors (ASIPs). It presents an overview of the research being currently performed in the scope of the European project ASAM of the ARTEMIS program. The paper briefly presents the results of our analysis of the main challenges to be faced in the design of such heterogeneous MPSoCs. It explains which system, design, and electronic design automation (EDA) concepts seem to be adequate to address the challenges and solve the problems. Finally, it discusses the ASAM design-flow, its main stages and tools and their application to a real-life case study.

General information
State: Published
Authors: Jozwiak, L. (Ekstern), Lindwer, M. (Ekstern), Corvino, R. (Ekstern), Meloni, P. (Ekstern), Micconi, L. (Intern), Madsen, J. (Intern), Diken, E. (Ekstern), Gangadharan, D. (Intern), Jordans, R. (Ekstern), Pomata, S. (Ekstern), Pop, P. (Intern), Tuveri, G. (Ekstern), Raffo, L. (Ekstern), Notarangelo, G. (Ekstern)
Pages: 1002-1019
Publication date: 2013
Main Research Area: Technical/natural sciences

Publication information
Journal: Microprocessors and Microsystems
Volume: 37
Issue number: 8, Part C
ISSN (Print): 0141-9331
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 0.771 SJR 0.24
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 1.11 SJR 0.225 SNIP 0.822
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.25 SNIP 0.857 CiteScore 0.89
Web of Science (2015): Indexed yes
A Time-predictable Stack Cache

Real-time systems need time-predictable architectures to support static worst-case execution time (WCET) analysis. One architectural feature, the data cache, is hard to analyze when different data areas (e.g., heap allocated and stack allocated data) share the same cache. This sharing leads to less precise results of the cache analysis part of the WCET analysis. Splitting the data cache for different data areas enables composable data cache analysis. The WCET analysis tool can analyze the accesses to these different data areas independently. In this paper we present the design and implementation of a cache for stack allocated data. Our port of the LLVM C++ compiler supports the management of the stack cache. The combination of stack cache instructions and the hardware implementation of the stack cache is a further step towards time-predictable architectures.
A Time-predictable Stack Cache

Real-time systems need time-predictable architectures to support static worst-case execution time (WCET) analysis. One architectural feature, the data cache, is hard to analyze when different data areas (e.g., heap allocated and stack allocated data) share the same cache. This sharing leads to less precise results of the cache analysis part of the WCET analysis. Splitting the data cache for different data areas enables composable data cache analysis. The WCET analysis tool can analyze the accesses to these different data areas independently. In this paper we present the design and implementation of a cache for stack allocated data. Our port of the LLVM C++ compiler supports the management of the stack cache. The combination of stack cache instructions and the hardware implementation of the stack cache is a further step towards time predictable architectures.

BCI using imaginary movements: The simulator

Over the past two decades, much progress has been made in the rapidly evolving field of Brain Computer Interface (BCI). This paper presents a novel concept: a BCI-simulator, which has been developed for the Hex-O-Spell interface, using the sensory motor rhythms (SMR) paradigm. With the simulator, it is possible to evaluate how the model parameters such as error classifications, delay between classifications and success rate affect the communication rate. Another advantage of the simulator is that it allows us to study for more classes than most online BCI systems which are limited to only two classes. Results show that the BCI simulator is able to give a deeper understanding of the feedback systems. We also find that a 3-class system is more efficient than a 2-class system if it obtains a success rate of at least 55% of the 2-class system.
Biochemical Application Compilation and Architecture Synthesis for Fault-Tolerant Digital Microfluidic Biochips

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Alister, M. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Number of pages: 1
Publication date: 2013
Event: Poster session presented at Lab-on-a-Chip World Congress, San Diego, CA, United States.
Main Research Area: Technical/natural sciences
Electronic versions:
LabOnChip_A1_Landscape.pdf

Chip-Multiprocessor Hardware Locks for Safety-Critical Java
Accessing shared resources in multicore systems is usually protected by a software locking mechanism, which itself is implemented through atomic operations. This can result in a large synchronization overhead, which, in the context of real-time systems, increases the worst-case execution time and may void a task set's schedulability. In this paper we present a hardware locking mechanism to reduce the synchronization overhead. The solution is implemented for the chip-multiprocessor version of the Java Optimized Processor in the context of safety-critical Java. The implementation is compared to a software solution. The performance and the hardware cost are evaluated.

Control Synthesis for the Flow-Based Microfluidic Large-Scale Integration Biochips
In this paper we are interested in flow-based microfluidic biochips, which are able to integrate the necessary functions for biochemical analysis on-chip. In these chips, the flow of liquid is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, mixers, and multiplexers, can be built. In this paper we propose, for the first time to our knowledge, a top-down control synthesis framework for the flow-based biochips. Starting from a given biochemical application and a biochip architecture, we synthesize the control logic that is used by the biochip controller to automatically execute the biochemical application. We also propose a control pin count minimization scheme aimed at efficiently utilizing chip area, reducing macro-assembly around the chip and enhancing chip scalability. We have evaluated our approach using both real-life applications and synthetic benchmarks.
Data cache organization for accurate timing analysis
Caches are essential to bridge the gap between the high latency main memory and the fast processor pipeline. Standard processor architectures implement two first-level caches to avoid a structural hazard in the pipeline: an instruction cache and a data cache. For tight worst-case execution times it is important to classify memory accesses as either cache hit or cache miss. The addresses of instruction fetches are known statically and static cache hit/miss classification is possible for the instruction cache. The access to data that is cached in the data cache is harder to predict statically. Several different data areas, such as stack, global data, and heap allocated data, share the same cache. Some addresses are known statically, other addresses are only known at runtime. With a standard cache organization all those different data areas must be considered by worst-case execution time analysis. In this paper we propose to split the data cache for the different data areas. Data cache analysis can be performed individually for the different areas. Access to an unknown address in the heap does not destroy the abstract cache state for other data areas. Furthermore, we propose to use a small, highly associative cache for the heap area. We designed and implemented a static analysis for this cache, and integrated it into a worst-case execution time analysis tool.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Vienna University of Technology
Authors: Schoeberl, M. (Intern), Huber, B. (Ekstern), Puffitsch, W. (Intern)
Pages: 1-28
Publication date: 2013
Main Research Area: Technical/natural sciences

Publication information
Journal: Real-Time Systems
Volume: 49
Issue number: 1
ISSN (Print): 0922-6443
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 2.237 SJR 0.257
Web of Science (2017): Indexed yes
BFI (2016): BFI-level 2
Scopus rating (2016): CiteScore 2.26 SJR 0.392 SNIP 1.703
BFI (2015): BFI-level 2
Scopus rating (2015): SJR 0.407 SNIP 1.904 CiteScore 1.85
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 2
Detecting and Preventing Beacon Replay Attacks in Receiver-Initiated MAC Protocols for Energy Efficient WSNs

In receiver-initiated MAC protocols for Wireless Sensor Networks (WSNs), communication is initiated by the receiver of the data through beacons containing the receiver's identity. In this paper, we consider the case of a network intruder that captures and replays such beacons towards legitimate nodes, pretending to have a fake identity within the network. To prevent this attack we propose RAP, a challenge-response authentication protocol that is able to detect and prevent the beacon replay attack. The effectiveness of the protocol is formally verified using OFMC and ProVerif. Furthermore, we provide an analysis that highlights the trade-offs between the energy consumption and the level of security, defined as the resilience of the protocol to space exhaustion.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Language-Based Technology
Authors: Di Mauro, A. (Intern), Fafoutis, X. (Intern), Mödersheim, S. A. (Intern), Dragoni, N. (Intern)
Pages: 1-16
Publication date: 2013
Dynamic allocation and admission policies for QoS-aware provisioning systems

We present an architecture of a hosting system consisting of a set of hosted web services subject to QoS constraints, and a certain number of servers used to run user's demand. The traffic is session-based, while provider and users agree on SLAs specifying the expected level of service performance such that the service provider is liable to compensate his/her customers if the level of performance is not satisfactory. The system is driven by a utility function which tries to optimise the average earned revenue per unit time. The middleware collects demand and performance statistics, and estimates traffic parameters in order to make dynamic decisions concerning server allocation and admission control. We empirically evaluate the effects of admission policies, resource allocation and service differentiation schemes on the achieved revenues, and we find that our system is robust enough to successfully deal with session-based traffic under different conditions.
ELB-trees an efficient and lock-free B-tree derivative

As computer systems scale in the number of processors, scalable data structures with good parallel performance become increasingly important. Lock-free data structures promise such improved parallel performance at the expense of higher algorithmic complexity and higher sequential execution time overhead. All lock-free data structures are based on simple atomic operations that, though supported by modern processors, are expensive in execution time. We present a lock-free data structure, ELB-trees, which under certain assumptions can be used as multimaps as well as priority queues. Specifically it cannot store duplicate key-value pairs, and it is not linearizable. Compared to existing data structures, ELB-trees require fewer atomic operations leading to improved performance. We measure the parallel performance of ELB-trees using a set of benchmarks and observe that ELB-trees are up to almost 30 times faster than library multimap implementations.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Language-Based Technology
Authors: Bonnichsen, L. F. (Intern), Karlsson, S. (Intern), Probst, C. W. (Intern)
Number of pages: 10
Publication date: 2013

Explicit Precedence Constraints in Safety-Critical Java

Safety-critical Java (SCJ) aims at making the amenities of Java available for the development of safety-critical applications. The multi-rate synchronous language Prelude facilitates the specification of the communication and timing requirements of complex real-time systems. This paper combines Prelude and SCJ in order to benefit from the advantages of both approaches. An obstacle we encountered when combining these approaches was that Prelude relies on a scheduler that observes precedence constraints, but SCJ does not provide adequate support for this. Therefore, we propose an extension of SCJ to provide explicit support for precedence constraints. We present the considerations behind the design of this extension and discuss our experiences with a first prototype implementation based on the SCJ implementation of the Java Optimized Processor.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Office National d'Études et Recherches Aéospatiales
Formal methods for design and simulation of embedded systems

Cyber physical systems (CPSs) are present in many variants in our daily life. The complexity of developing a CPS is quickly increasing and the interaction between different CPSs is increasingly important. The interaction of the systems is becoming more and more fluent and seamless.

This thesis presents the development of a formal systems modelling (ForSyDe) framework for modelling CPSs. The formalism of the framework makes computer aided design (CAD) a possibility for developing CPSs. The framework consists of four models of computation (MoCs): synchronous (SY), synchronous data flow (SDF), discrete event (DE), and continuous time (CT).

Usage of the framework is demonstrated with two use cases. A company use case featuring a hearing aid calibration device and the distributed energy harvesting aware routing (DEHAR) algorithm for wireless sensor networks (WSNs). These two use cases illustrate different design challenges. With the ForSyDe framework, the use cases are expressed as homogeneous and heterogeneous models.

The company use case illustrates that the ForSyDe framework handles systems with well defined interactions very well. The WSN use case illustrates that networked systems with complex interaction are more challenging to express naturally, yet the ForSyDe framework is able to express such systems.

Fourier Transform Spectrometer Controller for Partitioned Architectures

The current trend in spacecraft computing is to integrate applications of different criticality levels on the same platform using no separation. This approach increases the complexity of the development, verification and integration processes, with an impact on the whole system life cycle. Researchers at ESA and NASA advocated for the use of partitioned architecture to reduce this complexity. Partitioned architectures rely on platform mechanisms to provide robust temporal and spatial separation between applications. Such architectures have been successfully implemented in several industries, such as avionics and automotive. In this paper we investigate the challenges of developing and the benefits of
integrating a scientific instrument, namely a Fourier Transform Spectrometer, in such a partitioned architecture.

**General information**

State: Published

Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, NASA Jet Propulsion Laboratory, Designs & Prototypes Ltd., Quant Engineering LLC


Number of pages: 11

Publication date: 2013

**Functional Programming Using F#**

This comprehensive introduction to the principles of functional programming using F# shows how to apply basic theoretical concepts to produce succinct and elegant programs. It demonstrates the role of functional programming in a wide spectrum of applications including databases and systems. Coverage also includes advanced features in the .NET library, the imperative features of F# and topics such as text processing, sequences, computation expressions and asynchronous computation. With a broad spectrum of examples and exercises, the book is perfect for courses in functional programming and for self-study. Enhancing its use as a text is an accompanying website with downloadable programs, lecture slides, a mini-projects and links to further F# sources.

**Hardware support for CSP on a Java chip multiprocessor**

Due to memory bandwidth limitations, chip multiprocessors (CMPs) adopting the convenient shared memory model for their main memory architecture scale poorly. On-chip core-to-core communication is a solution to this problem, that can lead to further performance increase for a number of multithreaded applications. Programmatically, the Communicating Sequential Processes (CSPs) paradigm provides a sound computational model for such an architecture with message based communication. In this paper we explore hardware support for CSP in the context of an embedded Java CMP. The hardware support for CSP are on-chip communication channels, implemented by a ring-based network-on-chip (NoC), to reduce the memory bandwidth pressure on the shared memory. The presented solution is scalable and also specific for our limited resources and real-time predictability requirements. CMP architectures of three to eight processors were implemented and tested on both Altera (EP1C12, EP2C70) and Xilinx (XC3S1200e) FPGAs, showing that the NoC accounts for under 9% of the total device area used by the system. Compared to shared memory-based communication, our NoC-based solution is between 1.7 and 9.3 times faster for raw data transfer, depending on the communication and
memory configuration. Application speed-up, on the other hand, is highly dependent on the type of processing, as our measurements show.

**General information**
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Lund University
Authors: Gruian, F. (Ekstern), Schoeberl, M. (Intern)
Pages: 472-481
Publication date: 2013
Main Research Area: Technical/natural sciences

**Publication information**
Journal: Microprocessors and Microsystems
Volume: 37
Issue number: 4-5
ISSN (Print): 0141-9331
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 0.771 SJR 0.24
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 1
Scopus rating (2016): CiteScore 1.11 SJR 0.225 SNIP 0.822
Web of Science (2016): Indexed yes
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.25 SNIP 0.857 CiteScore 0.89
Web of Science (2015): Indexed yes
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.236 SNIP 1.057 CiteScore 0.97
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.225 SNIP 1.182 CiteScore 1.02
ISI indexed (2013): ISI indexed yes
Web of Science (2013): Indexed yes
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.214 SNIP 0.729 CiteScore 0.94
ISI indexed (2012): ISI indexed yes
BFI (2011): BFI-level 1
Scopus rating (2011): SJR 0.214 SNIP 0.797 CiteScore 0.99
ISI indexed (2011): ISI indexed yes
Web of Science (2011): Indexed yes
BFI (2010): BFI-level 1
Scopus rating (2010): SJR 0.255 SNIP 0.913
BFI (2009): BFI-level 1
Scopus rating (2009): SJR 0.223 SNIP 0.804
BFI (2008): BFI-level 1
Scopus rating (2008): SJR 0.256 SNIP 0.885
Scopus rating (2007): SJR 0.327 SNIP 0.841
Scopus rating (2006): SJR 0.372 SNIP 0.548
Scopus rating (2005): SJR 0.171 SNIP 0.671
Scopus rating (2004): SJR 0.208 SNIP 0.744
Scopus rating (2003): SJR 0.238 SNIP 0.99
Scopus rating (2002): SJR 0.227 SNIP 0.659
Scopus rating (2001): SJR 0.205 SNIP 0.536
Scopus rating (2000): SJR 0.131 SNIP 0.35
Scopus rating (1999): SJR 0.17 SNIP 0.255
Hierarchical DSE for multi-ASIP platforms

This work proposes a hierarchical Design Space Exploration (DSE) for the design of multi-processor platforms targeted to specific applications with strict timing and area constraints. In particular, it considers platforms integrating multiple Application Specific Instruction Set Processors (ASIPs) and each ASIP is automatically synthesized and tuned for a specific set of tasks. The definition of the platform (number of processors and their interconnection) and of the micro-architecture of each single ASIP are tightly coupled. Tasks can be allocated to the different ASIPs only knowing their performance and therefore the ASIP micro-architecture. At the same time an ASIP can be derived only knowing the functionality that it has to implement, i.e. the tasks that are assigned. We break this circular dependency with an iterative hierarchical DSE, applied at platform and micro-architecture level. We evaluate different platforms and micro-architecture alternatives to find a multi-ASIP platform targeted to the input application and able to meet the design constraints. We evaluate our design flow using a MJPEG encoder application.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technische Universiteit Eindhoven
Authors: Micconi, L. (Intern), Corvino, R. (Ekstern), Gangadharan, D. (Intern), Madsen, J. (Intern), Pop, P. (Intern), Jozwiak, L. (Ekstern)
Pages: 50-53
Publication date: 2013

Host publication information
Title of host publication: 2013 2nd Mediterranean Conference on Embedded Computing (MECO)
Publisher: IEEE
Main Research Area: Technical/natural sciences
Conference: 2nd Mediterranean Conference on Embedded Computing (MECO 2013), Budva, Montenegro, 15/06/2013 - 15/06/2013
DOIs:
10.1109/MECO.2013.6601379
Source: dtu
Source-ID: n::oai:DTIC-ART:iel/392401297::33652
Publication: Research - peer-review › Article in proceedings – Annual report year: 2013

Layout-Driven Post-Placement Techniques for Temperature Reduction and Thermal Gradient Minimization

With the continuing scaling of CMOS technology, on-chip temperature and thermal-induced variations have become a major design concern. To effectively limit the high temperature in a chip equipped with a cost-effective cooling system, thermal specific approaches, besides low power techniques, are necessary at the chip design level. The high temperature in hotspots and large thermal gradients are caused by the high local power density and the nonuniform power dissipation across the chip. With the objective of reducing power density in hotspots, we propose two placement techniques that spread cells in hotspots over a larger area. Increasing the area occupied by the hotspot directly reduces its power density, leading to a reduction in peak temperature and thermal gradient. To minimize the introduced overhead in delay and dynamic power, we maintain the relative positions of the coupling cells in the new layout. We compare the proposed methods in terms of temperature reduction, timing, and area overhead to the baseline method, which enlarges the circuit area uniformly. The experimental results showed that our methods achieve a larger reduction in both peak temperature and thermal gradient than the baseline method. The baseline method, although reducing peak temperature in most cases, has little impact on thermal gradient.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Oticon A/S, Politecnico di Torino
Authors: Liu, W. (Ekstern), Calimera, A. (Ekstern), Macii, A. (Ekstern), Macii, E. (Ekstern), Nannarelli, A. (Intern), Poncino, M. (Ekstern)
Pages: 406-418
Publication date: 2013
Main Research Area: Technical/natural sciences
Medium Access Control for Thermal Energy Harvesting in Advanced Metering Infrastructures
In this paper we investigate the feasibility of powering wireless metering devices, namely heat cost allocators, by thermal energy harvested from radiators. The goal is to take a first step toward the realization of Energy-Harvesting Advanced Metering Infrastructures (EH-AMIs). While traditional battery-powered devices have a limited amount of energy, energy harvesting can potentially provide an infinite amount of energy for continuous operating lifetimes, thus reducing the cost involved in installation and maintenance. The contribution of this work is twofold. First, we experimentally identify the potential energy that can be harvested from Low Surface Temperature (LST) radiators. The experiments are based on a developed Energy-Harvesting Heat Cost Allocator (EH-HCA) prototype. On the basis of this measured power budget, we model and analytically compare the currently used Medium Access Control (MAC) scheme of an industrial case study (IMR+) to a MAC scheme specifically designed for energy harvesting systems (ODMAC). Our analytical comparison shows the efficiency of the latter, as well as its ability to adapt to harvested ambient energy.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark, Brunata A/S
Authors: Vithanage, M. D. (Ekstern), Fafoutis, X. (Intern), Andersen, C. B. (Ekstern), Dragoni, N. (Intern)
Pages: 291-299
Publication date: 2013

Host publication information
Title of host publication: 2013 IEEE EUROCON
Publisher: IEEE
ISBN (Print): 978-1-4673-2232-4, 978-1-4673-2230-0
Main Research Area: Technical/natural sciences
Conference: IEEE Eurocon 2013, Zagreb, Croatia, 01/07/2013 - 01/07/2013
DOI:
10.1109/EUROCON.2013.6624999
Source: dtu
Source-ID: n:oai:DTIC-ART:iel/409253592::32723
Publication: Research - peer-review » Article in proceedings – Annual report year: 2013

Micro-transactions for concurrent data structures
Transactional memory is a promising technique for enforcing disciplined access to shared data in a multiprocessor system. Transactional memory simplifies the implementation of a variety of concurrent data structures. In this paper, we study the benefits of a modest, real-time aware, hardware implementation of transactional memory that we call micro-transactions. In particular, we argue that hardware support for micro-transactions allows us to efficiently implement certain data structures. Those data structures are difficult to realize with the atomic operations provided by stock hardware and provide real-time guarantees for those operations. Our main implementation platform is the Java Optimized Processor system, a field-programmable gate array (FPGA) implementation of the Java virtual machine, optimized for real-time Java. We report on the performance of data structures implemented with locks, atomic instructions, and micro-transactions. Our results suggest that transactional memory is an interesting alternative to traditional concurrency control mechanisms.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Purdue University
Authors: Meawad, F. (Ekstern), Iyer, K. (Ekstern), Schoeberl, M. (Intern), Vitek, J. (Ekstern)
Pages: 2252–2268
Publication date: 2013
Main Research Area: Technical/natural sciences

Publication information
Journal: Concurrency and Computation: Practice & Experience
Volume: 25
Issue number: 16
ISSN (Print): 1532-0626
Ratings:
BFI (2018): BFI-level 2
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 2
Scopus rating (2017): SNIP 0.76 SJR 0.282
Web of Science (2017): Indexed Yes
BFI (2016): BFI-level 2
MITHYS: Mind The Hand You Shake - Protecting Mobile Devices from SSL Usage Vulnerabilities

Recent studies have shown that a significant number of mobile applications, often handling sensitive data such as bank accounts and login credentials, suffers from SSL vulnerabilities. Most of the time, these vulnerabilities are due to improper use of the SSL protocol (in particular, in its handshake phase), resulting in applications exposed to man-in-the-middle attacks. In this paper, we present MITHYS, a system able to: (i) detect applications vulnerable to man-in-the-middle attacks, and (ii) protect them against these attacks. We demonstrate the feasibility of our proposal by means of a prototype implementation in Android, named MITHYSApp. A thorough set of experiments assesses the validity of our solution in detecting and protecting mobile applications from man-in-the-middle attacks, without introducing significant overheads. Finally, MITHYSApp does not require any special permissions nor OS modifications, as it operates at the application level. These features make MITHYSApp immediately deployable on a large user base.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Padua, Technical University of Denmark
Authors: Conti, M. (Ekstern), Dragoni, N. (Intern), Gottardo, S. (Ekstern)
Pages: 65-81
Modeling and Simulation Framework for Flow-Based Microfluidic Biochips

Microfluidic biochips are replacing the conventional biochemical analyzers and are able to integrate the necessary functions for biochemical analysis on-chip. In this paper we are interested in flow-based biochips, in which the fluidic flow is manipulated using integrated microvalves. By combining several microvalves, more complex units, such as micropumps, switches, mixers, and multiplexers, can be built. Such biochips are becoming increasingly complex, with thousands of components, but are still designed manually using a bottom-up full-custom design approach, which is extremely labor intensive and error prone. In this paper, we present an Integrated Development Environment (IDE), which addresses (i) schematic capture of the biochip architecture and biochemical application, (ii) logic simulation of an application running on a biochip, and is able to integrate the high level synthesis tasks we have developed for the top-down design of flow-based biochips. We show how the IDE can be used to design biochips for several applications.

Module-Based Synthesis of Digital Microfluidic Biochips with Droplet-Aware Operation Execution

Microfluidic biochips represent an alternative to conventional biochemical analyzers. A digital biochip manipulates liquids not as continuous flow, but as discrete droplets on a two-dimensional array of electrodes. Several electrodes are dynamically grouped to form a virtual device, on which operations are executed by moving the droplets. So far, researchers have ignored the locations of droplets inside devices, considering that all the electrodes forming the device are occupied throughout the operation execution. In this article, we consider a droplet-aware execution of microfluidic operations, which means that we know the exact position of droplets inside the modules at each time-step. We propose a Tabu Search-based metaheuristic for the synthesis of digital biochips with droplet-aware operation execution. Experimental results show that our approach can significantly reduce the application completion time, allowing us to use smaller area biochips and thus reduce costs.
Multi-ASIP Platform Synthesis for Event-Triggered Applications with Cost/Performance Trade-offs

In this paper, we propose a technique to synthesize a cost-efficient distributed platform consisting of multiple Application Specific Instruction Set Processors (multi-ASIPs) running applications with strict timing constraints. Multi-ASIP platform synthesis is a non-trivial task for two reasons. Firstly, we need to know the WCET of tasks in target applications to derive platforms (including synthesized ASIPs) in which the tasks are schedulable. However, the WCET of tasks can be known only after the ASIPs are synthesized. We break this circular dependency by using a probability distribution of the WCET (further referred to as the WCET uncertainty model), which takes into account the underlying microarchitectural configurations for the ASIP implementation. Secondly, the datapath area of the multi-ASIPs synthesized is an important design factor that contributes significantly towards the overall cost of the platform. We propose an area estimation model and a WCET uncertainty model that consider the effect of task datapath similarity. Based on these two models, we support the designer in exploring cost/performance trade-offs during the platform synthesis. We propose an Evolutionary Algorithm-based approach to solve this multiobjective optimization problem. The proposed approach has been evaluated using several benchmarks and it provides a number of multi-ASIP platform solutions exploring the trade-offs in the cost/performance design space.
Multi-ASIP Platform Synthesis for Real-Time Applications

In this paper we are interested in deriving a distributed platform, composed of heterogeneous processing elements, targeted to applications that have strict timing constraints. We consider that the platform may use multiple Application Specific Instruction Set Processors (ASIPs). An ASIP is synthesized and tuned for a specific set of tasks (i.e., a task cluster). During design space exploration (DSE), we evaluate each platform solution visited in terms of its cost and performance, i.e., its ability to execute the applications such that they meet their timing constraints. To determine if the applications are schedulable, we have to know the worst-case execution time (WCET) of each task. However, we can determine the WCETs only after the ASIPs are synthesized, which is time consuming and therefore cannot be done during DSE. To address this circular dependency (the ASIPs depend on the task clustering, and the WCETs of tasks, used to determine schedulability, depend on how ASIPs are synthesized), we propose an uncertainty model for the WCETs, which captures the range of possible ASIP implementations. Based on this model, we synthesize a multi-ASIP platform, such that the applications have a high chance of being schedulable and the cost constraints imposed on the platform are fulfilled. We propose an Evolutionary Algorithm-based approach, which uses a novel stochastic schedulability analysis to solve this optimization problem. The proposed approach has been evaluated using several benchmarks.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Micconi, L. (Intern), Gangadharan, D. (Intern), Pop, P. (Intern), Madsen, J. (Intern)
Pages: 59-67
Publication date: 2013
Optimal scheduling of complex processes through stochastic model checking: An example from the baked goods industry

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Department of Management Engineering, Management Science, Production and Service Management
Authors: Herbert, L. T. (Intern), Hansen, Z. N. L. (Intern), Sharp, R. (Intern), Jacobsen, P. (Intern)
Publication date: 2013

Host publication information
Title of host publication: Proceedings of the 3rd International Conference on Modelling and Management of Engineering Processes
Main Research Area: Technical/natural sciences
Publication: Research - peer-review › Article in proceedings – Annual report year: 2013

Optimisation of BPMN Business Models via Model Checking
We present a framework for the optimisation of business processes modelled in the business process modelling language BPMN, which builds upon earlier work, where we developed a model checking based method for the analysis of BPMN models. We define a structure for expressing optimisation goals for synthesized BPMN components, based on probabilistic computation tree logic and real-valued reward structures of the BPMN model, allowing for the specification of complex quantitative goals. We here present a simple algorithm, inspired by concepts from evolutionary algorithms, which iteratively generates candidate improved processes based on the fittest of the previous generation. The evaluation of the fitness of each candidate in a generation is performed via model checking, detailed in previous work. At each iteration, this allows the determination of the precise numerical evaluation of the performance of a candidate in terms of the specified goals. A discussion of this method's application, and the degree of optimization which is possible, is illustrated using an example drawn from the healthcare industry.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Herbert, L. T. (Intern), Sharp, R. (Intern)
Number of pages: 10
Pages: DETC2013-13047
Publication date: 2013

Host publication information
Publisher: American Society of Mechanical Engineers
Main Research Area: Technical/natural sciences
Source: dtu
Source-ID: u::9447
Publication: Research - peer-review › Article in proceedings – Annual report year: 2013

Precise Quantitative Analysis of Probabilistic Business Process Model and Notation Workflows
We present a framework for modeling and analysis of real-world business workflows. We present a formalized core subset of the business process modeling and notation (BPMN) and then proceed to extend this language with probabilistic
nondeterministic branching and general-purpose reward annotations. We present an algorithm for the translation of such models into Markov decision processes (MDP) expressed in the syntax of the PRISM model checker. This enables precise quantitative analysis of business processes for the following properties: transient and steady-state probabilities, the timing, occurrence and ordering of events, reward-based properties, and best- and worst-case scenarios. We develop a simple example of medical workflow and demonstrate the utility of this analysis in accurate provisioning of drug stocks. Finally, we suggest a path to building upon these techniques to cover the entire BPMN language, allow for more complex annotations and ultimately to automatically synthesize workflows by composing predefined subprocesses, in order to achieve a configuration that is optimal for parameters of interest.

**General information**

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Herbert, L. T. (Intern), Sharp, R. (Intern)
Number of pages: 9
Pages: 011007
Publication date: 2013
Main Research Area: Technical/natural sciences

**Publication information**

Journal: Journal of Computing and Information Science in Engineering
Volume: 13
Issue number: 1
ISSN (Print): 1530-9827
Ratings:

- BFI (2018): BFI-level 1
- Web of Science (2018): Indexed yes
- BFI (2017): BFI-level 1
- Scopus rating (2017): SNIP 1.257 SJR 0.627
- Web of Science (2017): Indexed Yes
- BFI (2016): BFI-level 1
- Scopus rating (2016): SJR 0.543 SNIP 0.892 CiteScore 1.44
- BFI (2015): BFI-level 1
- Scopus rating (2015): SJR 0.455 SNIP 0.985 CiteScore 0.96
- BFI (2014): BFI-level 1
- Scopus rating (2014): SJR 0.538 SNIP 1.221 CiteScore 1.01
- BFI (2013): BFI-level 1
- Scopus rating (2013): SJR 0.656 SNIP 1.231 CiteScore 1.22
- ISI indexed (2013): ISI indexed yes
- Web of Science (2013): Indexed yes
- BFI (2012): BFI-level 1
- Scopus rating (2012): SJR 0.519 SNIP 1.142 CiteScore 0.72
- ISI indexed (2012): ISI indexed yes
- BFI (2011): BFI-level 1
- Scopus rating (2011): SJR 0.415 SNIP 1.028 CiteScore 0.93
- ISI indexed (2011): ISI indexed yes
- BFI (2010): BFI-level 1
- Scopus rating (2010): SJR 0.415 SNIP 1.246
- BFI (2009): BFI-level 1
- Scopus rating (2009): SJR 0.601 SNIP 0.997
- BFI (2008): BFI-level 1
- Scopus rating (2008): SJR 0.534 SNIP 0.914
- Scopus rating (2007): SJR 0.449 SNIP 1.134
- Web of Science (2007): Indexed yes
- Scopus rating (2006): SJR 0.466 SNIP 1.022
- Scopus rating (2005): SJR 0.377 SNIP 0.987
- Scopus rating (2004): SJR 0.689 SNIP 1.189
- Scopus rating (2003): SNIP 0.822 SJR 0.39
- Scopus rating (2002): SNIP 1.202
Quality-Driven Model-Based Design of MultiProcessor Embedded Systems for Highlydemanding Applications

The recent spectacular progress in modern nano-dimension semiconductor technology enabled implementation of a complete complex multi-processor system on a single chip (MPSoC), global networking and mobile wire-less communication, and facilitated a fast progress in these areas. New important opportunities have been created. The traditional applications can be served much better and numerous new sorts of embedded systems became technologically feasible and economically justified. Various monitoring, control, communication or multi-media systems that can be put on or embedded in (mobile, poorly accessible or distant) objects, installations, machines or devices, or even implanted in human or animal body can serve as examples. However, many of the modern embedded application impose very stringent functional and parametric demands. Moreover, the spectacular advances in microelectronics introduced unusual silicon and system complexity. The combination of the huge complexity with the stringent application requirements results in numerous serious design and development challenges, such as: accounting in design for more aspects and changed relationships among aspects, complex multi-objective MPSoC optimization, adequate resolution of numerous complex design tradeoffs, reduction of the design productivity gap for the increasingly complex and sophisticated systems, reduction of the time-to market and development costs without compromising the system quality, etc. These challenges cannot be well addressed without an adequate system and design methodology adaptation. The adequate system and design paradigms to solve the problems seem to be the paradigms of: life-inspired systems, and quality-driven design. The first part of the tutorial is devoted to discussion of the issues and challenges in development of contemporary and future embedded systems and introduction of the quality-driven model-based design methodology based on the paradigms of life-inspired systems and quality-driven design earlier proposed by the first presenter of this tutorial. Subsequently, the actual industrial Intel's ASIP-based MPSoC technology is introduced, and situation, trends and problems are discussed in the area of heterogeneous MPSoCs based on adaptable ASIPs and hardware accelerators for highly-demanding applications.

Router Designs for an Asynchronous Time-Division-Multiplexed Network-on-Chip

In this paper we explore the design of an asynchronous router for a time-division-multiplexed (TDM) network-on-chip (NOC) that is being developed for a multi-processor platform for hard real-time systems. TDM inherently requires a common time reference, and existing TDM-based NOC designs are either synchronous or mesochronous, but both approaches have their limitations: a globally synchronous NOC is no longer feasible in today's sub micron technologies and a mesochronous NOC requires special FIFO-based synchronizers in all input ports of all routers in order to accommodate for clock phase differences. This adds hardware complexity and increases area and power consumption. We propose to use asynchronous routers in order to achieve a simpler, more robust and globally-asynchronous NOC, and this represents an unexplored point in the design space. The paper presents a range of alternative router designs. All routers have been synthesized for a 65nm CMOS technology, and the paper reports post-layout figures for area, speed and energy and compares the asynchronous designs with an existing mesochronous clocked router. The results show that an asynchronous router is 2 times smaller, marginally slower and with roughly the same energy consumption, while offering a robust solution to the clock distribution problem. The paper further explores “clock-gating” of the individual pipeline stages in the asynchronous routers, and shows that this can lead to significant power savings.
Social Networks and Collective Intelligence: A Return to the Agora

Nowadays, acquisition of trustable information is increasingly important in both professional and private contexts. However, establishing what information is trustable and what is not, is a very challenging task. For example, how can information quality be reliably assessed? How can sources' credibility be fairly assessed? How can gatekeeping processes be found trustworthy when filtering out news and deciding ranking and priorities of traditional media? An Internet-based solution to a human-based ancient issue is being studied, and it is called Polidoxa, from Greek "poly", meaning "many" or "several" and "doxa", meaning "common belief" or "popular opinion". This old problem will be solved by means of ancient philosophies and processes with truly modern tools and technologies. This is why this work required a collaborative and interdisciplinary joint effort from researchers with very different backgrounds and institutes with significantly different agendas. Polidoxa aims at offering: 1) a trust-based search engine algorithm, which exploits stigmergic behaviours of users' network, 2) a trust-based social network, where the notion of trust derives from network activity and 3) a holonic system for bottom-up self-protection and social privacy. By presenting the Polidoxa solution, this work also describes the current state of traditional media as well as newer ones, providing an accurate analysis of major search engines such as Google and social network (e.g., Facebook). The advantages that Polidoxa offers, compared to these, are also clearly detailed and motivated. Finally, a Twitter application (Polidoxa@twitter) which enables experimentation of basic Polidoxa principles is presented.

Static analysis of worst-case stack cache behavior

Utilizing a stack cache in a real-time system can aid predictability by avoiding interference that heap memory traffic causes on the data cache. While loads and stores are guaranteed cache hits, explicit operations are responsible for managing the
The behavior of these operations can be analyzed statically. We present algorithms that derive worst-case bounds on the latency-inducing operations of the stack cache. Their results can be used by a static WCET tool. By breaking the analysis down into subproblems that solve intra-procedural data-flow analysis and path searches on the call-graph, the worst-case bounds can be efficiently yet precisely determined. Our evaluation using the MiBench benchmark suite shows that only 37% and 21% of potential stack cache operations actually store to and load from memory, respectively. Analysis times are modest, on average running between 0.46s and 1.30s per benchmark, depending on the size of the stack cache.

Sustainable medium access control: Implementation and evaluation of ODMAC
Harvesting small-scale ambient energy constitutes a promising source of power for wireless embedded devices. Due to the unpredictable nature of the harvested energy, adaptive radio duty cycling can lead to a long-term sustainable operation. In energy constrained conditions, very low duty cycles are vital to guarantee the sustainability of the system; whereas, in the opposite case, the system should use the energy surplus to increase the application performance. In this paper, we implement and evaluate On-Demand MAC (ODMAC), the first receiver-initiated MAC protocol specifically designed for energy harvesting applications. In particular, we provide a basic yet fully operational implementation of ODMAC for the Texas Instruments' MSP430 microprocessor family. Furthermore, we verify the theoretical results of our previous work by achieving sustainable operation of an energy harvesting node in various cases of energy input using a real test-bed.

Sustainable Performance in Energy Harvesting - Wireless Sensor Networks
In this practical demo we illustrate the concept of “sustainable performance” in Energy-Harvesting Wireless Sensor Networks (EH-WSNs). In particular, for different classes of applications and under several energy harvesting scenarios, we show how it is possible to have sustainable performance when nodes in the network are powered by ambient energy.
Synthetic Aperture Radar Data Processing on an FPGA Multi-Core System

Synthetic aperture radar, SAR, is a high resolution imaging radar. The direct back-projection algorithm allows for a precise SAR output image reconstruction and can compensate for deviations in the flight track of airborne radars. Often graphic processing units, GPUs are used for data processing as the back-projection algorithm is computationally expensive and highly parallel. However, GPUs may not be an appropriate solution for applications with strictly constrained space and power requirements. In this paper, we describe how we map a SAR direct back-projection application to a multi-core system on an FPGA. The fabric consisting of 64 processor cores and 2D mesh interconnect utilizes 60% of the hardware resources of a Xilinx Virtex-7 device with 550 thousand logic cells and consumes about 10 watt. We apply software pipelining to hide memory latency and reduce the hardware footprint by 14%. We show that the system provides real-time processing of a SAR application that maps a 3000m wide area with a resolution of 2x2 meters.
Task Based Programming on Embedded Multicores

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schleuniger, P. (Intern), Karlsson, S. (Intern)
Number of pages: 1
Publication date: 2013
Event: Poster session presented at 8th International Conference on High-Performance and Embedded Architectures and Compilers, Berlin, Germany.
Main Research Area: Technical/natural sciences
Electronic versions: hipeac13.pdf
Source: PublicationPreSubmission
Source-ID: 104397805
Publication: Research › Poster – Annual report year: 2014

The hardness of the functional orientation 2-color problem
We consider the Functional Orientation 2-Color problem, which was introduced by Valiant in his seminal paper on holographic algorithms [SIAM J. Comput. 37(5) (2008), 1565-1594]. For this decision problem, Valiant gave a polynomial time holographic algorithm for planar graphs of maximum degree 3, and showed that the problem is NP-complete for planar graphs of maximum degree 10. A recent result on defective graph coloring by Corrêa et al. [Australas. J. Combin. 43 (2009), 219-230] implies that the problem is already hard for planar graphs of maximum degree 8. Together, these results leave open the hardness question for graphs of maximum degree between 4 and 7. We close this gap by showing that the answer is always yes for arbitrary graphs of maximum degree 5, and that the problem is NP-complete for planar graphs of maximum degree 6. Moreover, for graphs of maximum degree 5, we note that a linear time algorithm for finding a solution exists.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Algorithms and Logic, Embedded Systems Engineering
Authors: Stöckel, M. (Ekstern), Vildhøj, H. W. (Intern), Bøg, S. (Intern)
Pages: 225-234
Publication date: 2013
Main Research Area: Technical/natural sciences

Publication information
Journal: Australasian Journal of Combinatorics
Volume: 56
ISSN (Print): 1034-4942
Ratings:
BFI (2018): BFI-level 1
Web of Science (2018): Indexed yes
BFI (2017): BFI-level 1
Scopus rating (2017): SNIP 0.709 SJR 0.547
BFI (2016): BFI-level 1
Scopus rating (2016): SJR 0.42 SNIP 0.679 CiteScore 0.36
BFI (2015): BFI-level 1
Scopus rating (2015): SJR 0.524 SNIP 0.943 CiteScore 0.42
BFI (2014): BFI-level 1
Scopus rating (2014): SJR 0.316 SNIP 0.487 CiteScore 0.25
BFI (2013): BFI-level 1
Scopus rating (2013): SJR 0.369 SNIP 0.491 CiteScore 0.32
ISI indexed (2013): ISI indexed no
BFI (2012): BFI-level 1
Scopus rating (2012): SJR 0.594 SNIP 0.709 CiteScore 0.39
ISI indexed (2012): ISI indexed no
BFI (2011): BFI-level 1
Scopus rating (2011): SJR 0.414 SNIP 0.695 CiteScore 0.28
ISI indexed (2011): ISI indexed no
Truncated multipliers through power-gating for degrading precision arithmetic

When reducing the power dissipation of resource-constrained electronic systems is a priority, some precision can be traded-off for lower power consumption. In signal processing, it is possible to have an acceptable quality of the signal even introducing some errors. In this work, we apply power-gating to multipliers to obtain a programmable truncated multiplier. The method consists in disabling the least-significant columns of the multiplier by power-gating logic in the partial products generation and accumulation array.

General information

State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, University of Roma 'Tor Vergata', Politecnico di Torino
Authors: Albicocco, P. (Ekstern), Cardarilli, G. C. (Ekstern), Nannarelli, A. (Intern), Petricca, M. (Ekstern), Re, M. (Ekstern)
Pages: 2172-2176
Publication date: 2013

Host publication information

Title of host publication: Proceedings of 2013 Asilomar Conference on Signals, Systems and Computers
Publisher: IEEE
ISBN (Print): 978/1/4799/2390/8
Main Research Area: Technical/natural sciences
Bioengineering, Communication, Networking and Broadcast Technologies, Components, Circuits, Devices and Systems, Computing and Processing, Signal Processing and Analysis, Clocks, Delays, Digital signal processing, Finite impulse response filters, Layout, Logic gates, Power dissipation
DOIs: 10.1109/ACSSC.2013.6810694

Tutorial: Digital microfluidic biochips: Towards hardware/software co-design and cyber-physical system integration

This tutorial will first provide an overview of typical bio-molecular applications (market drivers) such as immunoassays, DNA sequencing, clinical chemistry, etc. Next, microarrays and various microfluidic platforms will be discussed. The next part of the tutorial will focus on electro-wetting-based digital micro-fluidic biochips. The key idea here is to manipulate liquids as discrete droplets. A number of case studies based on representative assays and laboratory procedures will be interspersed in appropriate places throughout the tutorial. Basic concepts in micro-fabrication techniques will also be discussed. Attendees will next learn about CAD and reconfiguration aspects of digital microfluidic biochips. Synthesis tools will be described to map assay protocols from the lab bench to a droplet-based microfluidic platform and generate an optimized schedule of bioassay operations, the binding of assay operations to functional units, and the layout and droplet-flow paths for the biochip. The role of the digital microfluidic platform as a "programmable and reconfigurable processor" for biochemical applications will be highlighted. Cyber-physical integration using low-cost sensors and adaptive control,
software will be highlighted. Cost-effective testing techniques will be described to detect faults after manufacture and during field operation. On-line and off-line reconfiguration techniques will be presented to easily bypass faults once they are detected. The problem of mapping a small number of chip pins to a large number of array electrodes will also be covered. With the availability of these tools, chip users and chip designers will be able to concentrate on the development and chip-level adaptation of nano-scale bioassays (higher productivity), leaving implementation details to CAD tools.

**General information**

State: Published  
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, National Taiwan University, National Chiao Tung University  
Authors: Ho, T. (Ekstern), Huang, J. (Ekstern), Pop, P. (Intern)  
Pages: 316-317  
Publication date: 2013

**Host publication information**

Title of host publication: 2013 IEEE 26th International SOC Conference (SOCC)  
Publisher: IEEE  
ISBN (Print): 978-1-4799-1166-0  
BFI conference series: Systems on Chip Conference (5010846)  
Main Research Area: Technical/natural sciences  
DOIs:  
10.1109/SOCC.2013.6749708  
Source: dtu  
Source-ID: n:oai:DTIC-ART:iel/434685663::38105  
Publication: Research - peer-review › Conference abstract in proceedings – Annual report year: 2014

**Analysis and Optimization of Mixed-Criticality Applications on Partitioned Distributed Architectures**

In this paper we are interested in mixed-criticality applications implemented using distributed heterogenous architectures, composed of processing elements (PEs) interconnected using the TTEthernet protocol. At the PE-level, we use partitioning, such that each application is allowed to run only within predefined time slots, allocated on each processor. At the communication-level, TTEthernet uses the concepts of virtual links for the separation of mixed-criticality messages. TTEthernet integrates three types of traffic: Time-Triggered (TT) messages, transmitted based on schedule tables, Rate Constrained (RC) messages, transmitted if there are no TT messages, and Best Effort (BE) messages. We assume that applications are scheduled using Static Cyclic Scheduling (SCS) or Fixed-Priority Preemptive Scheduling (FPS). We are interested in analysis and optimization methods and tools, which decide the mapping of tasks to PEs, the sequence and length of the time partitions on each PE and the schedule tables of the SCS tasks and TT messages, such that the applications are schedulable and the response times of FPS tasks and RC messages is minimized. We have proposed a Tabu Search-based meta-heuristic to solve this optimization problem, which has been evaluated using several benchmarks.

**General information**

State: Published  
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark  
Authors: Tamas-Selicean, D. (Intern), Marinescu, S. O. (Ekstern), Pop, P. (Intern)  
Number of pages: 6  
Publication date: 2012

**Host publication information**

Title of host publication: 2012 IET System Safety Conference  
Publisher: Institution of Engineering and Technology  
Main Research Area: Technical/natural sciences  
Conference: 2012 IET System Safety Conference, Edinburgh, United Kingdom, 15/10/2012 - 15/10/2012  
Electronic versions:  
dota_iet_2012.pdf  
DOIs:  
10.1049/cp.2012.1504  
Source: dtu  
Source-ID: u::6869  
Publication: Research - peer-review › Article in proceedings – Annual report year: 2013
Attacker Modelling in Ubiquitous Computing Systems

Within the last five to ten years we have experienced an incredible growth of ubiquitous technologies which has allowed for improvements in several areas, including energy distribution and management, health care services, border surveillance, secure monitoring and management of buildings, localisation services and many others. These technologies can be classified under the name of ubiquitous systems.

The term Ubiquitous System dates back to 1991 when Mark Weiser at Xerox PARC Lab first referred to it in writing. He envisioned a future where computing technologies would have been melted in with our everyday life. This future is visible to everyone nowadays: terms like smartphone, cloud, sensor, network etc. are widely known and used in our everyday life. But what about the security of such systems. Ubiquitous computing devices can be limited in terms of energy, computing power and memory. The implementation of cryptographic mechanisms that comes from classical communication systems could be too heavy for the resources of such devices, thus forcing the use of lighter security measures if any at all. The same goes for the implementation of security protocols. The protocols employed in classical communication systems were not designed for the ubiquitous environment, hence their security has to be proven again, leading to the definition of new protocols designed specifically to address new vulnerabilities introduced by the ubiquitous nature of the system.

Throughout the network security community this problem has been investigated for some time now and this has resulted in some lightweight cryptographic standards and protocols, as well as tools that make it possible for security properties of communication protocols which are typical of ubiquitous systems. However the abilities of the ubiquitous attacker remain somehow undefined and still under extensive investigation.

This Thesis explores the nature of the ubiquitous attacker with a focus on how she interacts with the physical world and it defines a model that captures the abilities of the attacker. Furthermore a quantitative implementation of the model is presented. This can be used by a security analyst as a supporting tool to analyse the security of an ubiquitous system and identify its weak parts. Most importantly this work is also useful for system designers, who wish to implement an effective secure solution while developing their system.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Papini, D. (Intern), Sharp, R. (Intern), Jensen, C. D. (Intern)
Number of pages: 182
Publication date: 2012

Publication information
Place of publication: Kgs. Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English

Series: IMM-PHD-2012
Number: 295
ISSN: 0909-3192
Main Research Area: Technical/natural sciences
Electronic versions:
Attacker_Modelling.pdf
Publication: Research › Ph.D. thesis – Annual report year: 2014

Direct Measurement of Power Dissipated by Monte Carlo Simulations on CPU and FPGA Platforms

In this technical report, we describe how power dissipation measurements on different computing platforms (a desktop computer and an FPGA board) are performed by using a Hall effect-based current sensor. The chosen application is a Monte Carlo simulation for European option pricing which is a popular algorithm used in financial computations. The Hall effect probe measurements complement the measurements performed on the core of the FPGA by a built-in Xilinx power monitoring system.

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Technical University of Denmark
Authors: Albicocco, P. (Ekstern), Papini, D. (Intern), Nannarelli, A. (Intern)
Number of pages: 12
Publication date: 2012

Publication information
Place of publication: Kongens Lyngby
Publisher: Technical University of Denmark (DTU)
Original language: English

Number: 2012-18
Parallelizing More Loops with Compiler Guided Refactoring
The performance of many parallel applications relies not on instruction-level parallelism but on loop-level parallelism. Unfortunately, automatic parallelization of loops is a fragile process; many different obstacles affect or prevent it in practice. To address this predicament we developed an interactive compilation feedback system that guides programmers in iteratively modifying their application source code. This helps leverage the compiler’s ability to generate loop-parallel code. We employ our system to modify two sequential benchmarks dealing with image processing and edge detection, resulting in scalable parallelized code that runs up to 8.3 times faster on an eightcore Intel Xeon 5570 system and up to 12.5 times faster on a quad-core IBM POWER6 system. Benchmark performance varies significantly between the systems. This suggests that semi-automatic parallelization should be combined with target-specific optimizations. Furthermore, comparing the first benchmark to manually-parallelized, handoptimized pthreads and OpenMP versions, we find that code generated using our approach typically outperforms the pthreads code (within 93-339%). It also performs competitively against the OpenMP code (within 75-111%). The second benchmark outperforms manually-parallelized and optimized OpenMP code (within 109-242%).

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering, Chalmers University of Technology, IBM Research Laboratory
Authors: Larsen, P. (Intern), Ladelsky, R. (Ekstern), Lidman, J. (Ekstern), McKee, S. A. (Ekstern), Karlsson, S. (Intern), Zaks, A. (Ekstern)
Pages: 410-419
Publication date: 2012

Host publication information
Title of host publication: 2012 41st International Conference on Parallel Processing (ICPP)
Publisher: IEEE
ISBN (Print): 978-1-4673-2508-0
Series: International Conference on Parallel Processing. Proceedings
 ISSN: 0190-3918
BFI conference series: International Conference on Parallel Processing (5000144)
Main Research Area: Technical/natural sciences
Conference: 41st International Conference on Parallel Processing (ICPP 2012), Pittsburgh, United States, 10/09/2012 - 10/09/2012
DOIs: 10.1109/ICPP.2012.48
Source: dtu
Source-ID: u::7185
Publication: Research - peer-review › Article in proceedings – Annual report year: 2012

Software Managed Cache for Parallel Systems

General information
State: Published
Organisations: Department of Applied Mathematics and Computer Science, Embedded Systems Engineering
Authors: Schleuniger, P. (Intern), Karlsson, S. (Intern)
Number of pages: 1
Publication date: 2012
Event: Poster session presented at 7th International Conference on High-Performance and Embedded Architectures and Compilers, Paris, France.
Main Research Area: Technical/natural sciences
Electronic versions:
hipeac12.pdf
Source: PublicationPreSubmission
Source-ID: 104397794
Publication: Research › Poster – Annual report year: 2014
System-Level Modeling and Synthesis Techniques for Flow-Based Microfluidic Very Large Scale Integration Biochips

Microfluidic biochips integrate different biochemical analysis functionalities on-chip and offer several advantages over the conventional biochemical laboratories. In this thesis, we focus on the flow-based biochips. The basic building block of such a chip is a valve which can be fabricated at very high densities, e.g., 1 million valves per cm². By combining these valves, more complex units such as mixers, switches, multiplexers can be built up and the technology is therefore referred to as microfluidic Very Large Scale Integration (mVLSI).

The manufacturing technology for the mVLSI biochips has advanced faster than Moore’s law. However, the design methodologies are still manual and bottom-up. Designers use drawing tools, e.g., AutoCAD, to manually design the chip. In order to run the experiments, applications are manually mapped onto the valves of the chips (analogous to exposure of gate-level details in electronic integrated circuits). Since mVLSI chips can easily have thousands of valves, the manual process can be very time-consuming, error-prone and result in inefficient designs and mappings.

We propose, for the first time to our knowledge, a top-down modeling and synthesis methodology for the mVLSI biochips. We propose a modeling framework for the components and the biochip architecture. Using these models, we present an architectural synthesis methodology (covering steps from the schematic design to the physical synthesis), generating an application-specific mVLSI biochip. We also propose a framework for mapping the biochemical applications onto the mVLSI biochips, binding and scheduling the operations and performing fluid routing. A control synthesis framework for determining the exact valve activation sequence required to execute the application is also proposed. In order to reduce the macro-assembly around the chip and enhance chip scalability, we propose an approach for the biochip pin count minimization. We also propose a throughput maximization scheme for the cell culture mVLSI biochips, saving time and reducing costs. We have extensively evaluated the proposed approaches using real-life case studies and synthetic benchmarks. The proposed framework is expected to facilitate programmability and automation, enabling the emergence of a large biochip market.

Timming Analysis of Mixed-Criticality Hard Real-Time Applications Implemented on Distributed Partitioned Architectures

In this paper we are interested in the timing analysis of mixed-criticality embedded real-time applications mapped on distributed heterogeneous architectures. Mixed-criticality tasks can be integrated onto the same architecture only if there is enough spatial and temporal separation among them. We consider that the separation is provided by partitioning, such that applications run in separate partitions, and each partition is allocated several time slots on a processor. Each partition can have its own scheduling policy. We are interested to determine the worst-case response times of tasks scheduled in partitions using fixed-priority preemptive scheduling. We have extended the state-of-the-art algorithms for schedulability analysis to take into account the partitions. The proposed algorithm has been evaluated using several synthetic and real-life benchmarks.